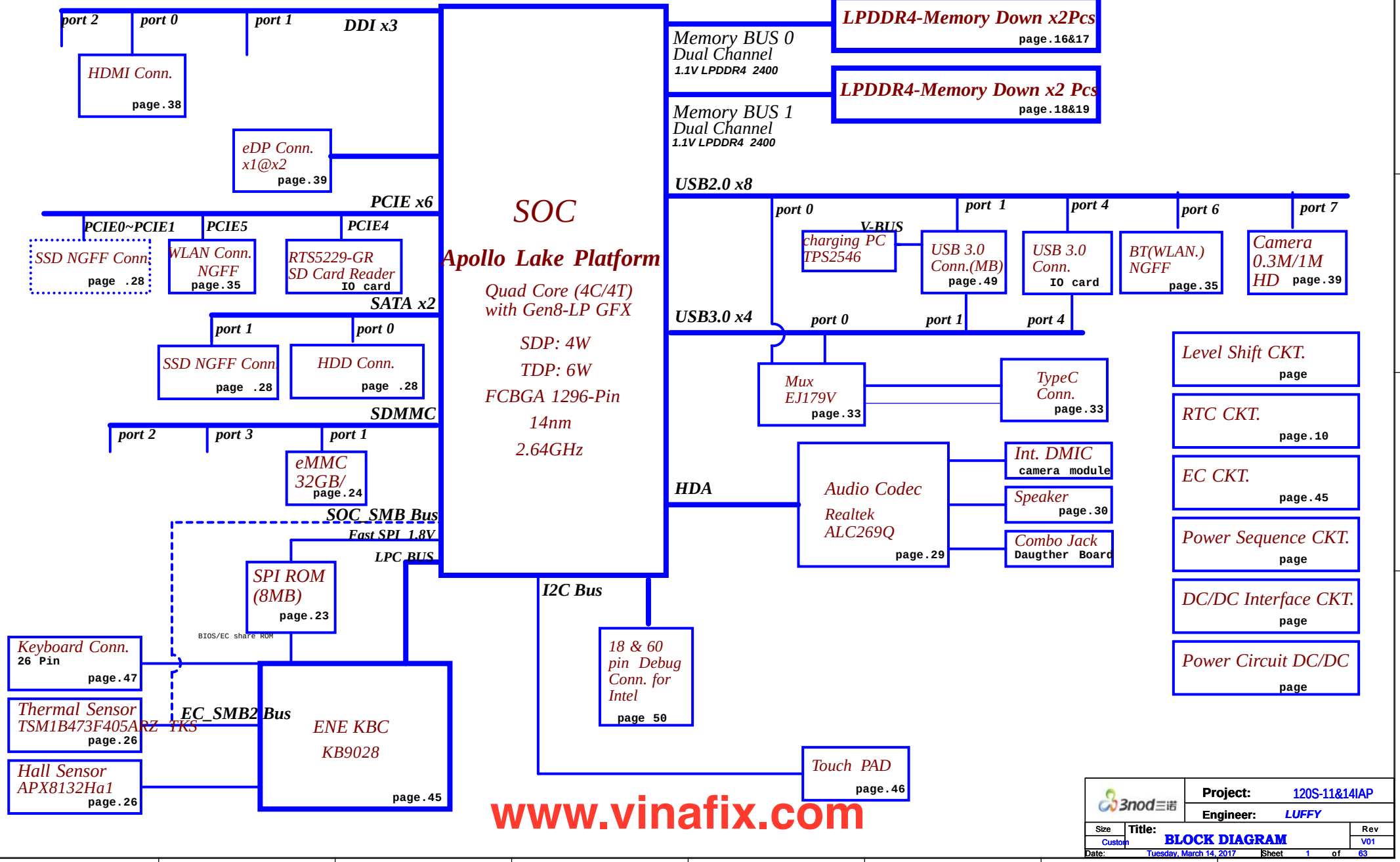
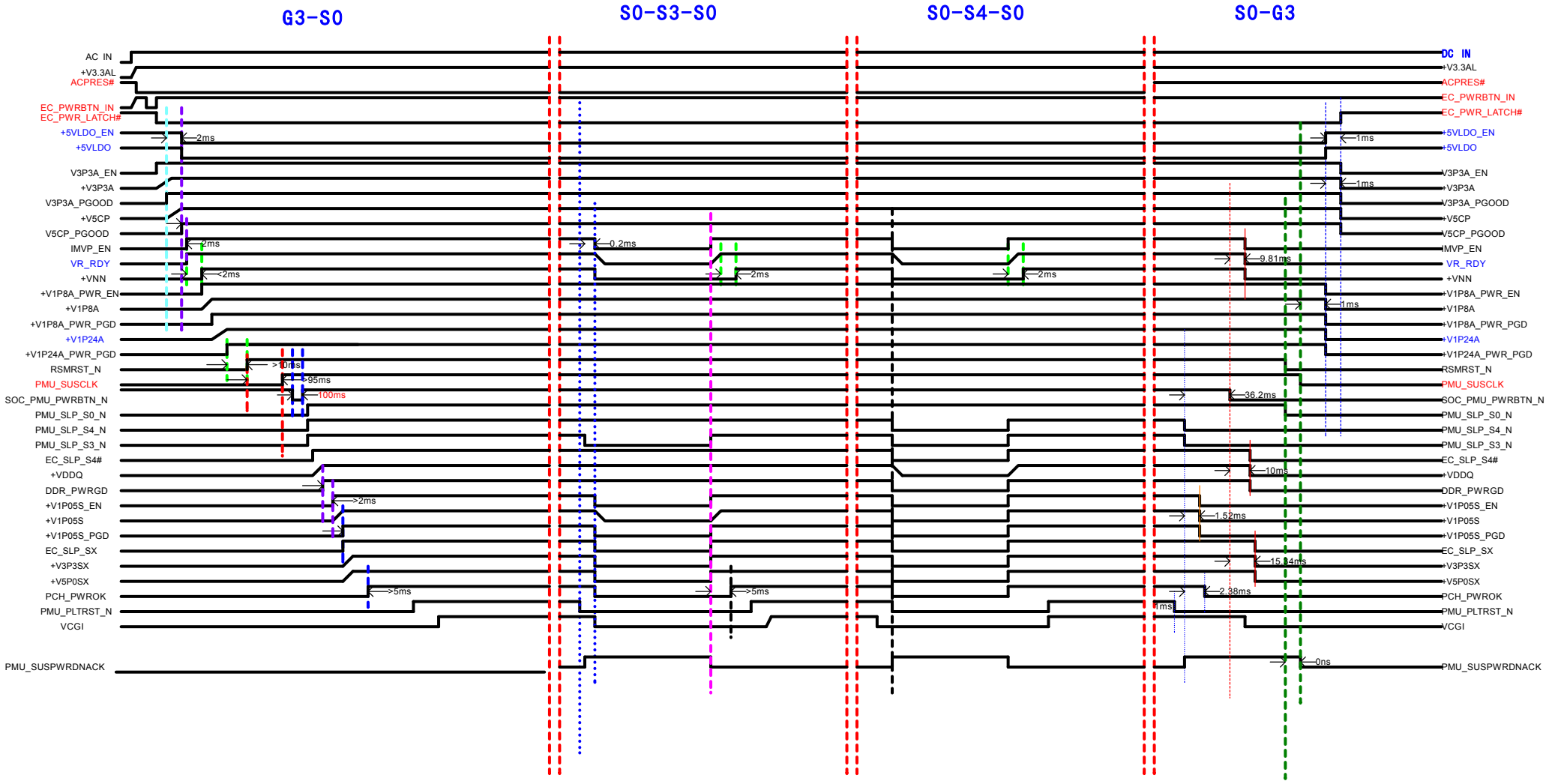
APL MRD FAB A



www.vinafix.com

3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: BLOCK DIAGRAM	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 1 of 63	



INTERNAL ONLY

BPAGE DRAWING

apl_ff.8A
Fri May 27 06:47:24 2016

3nod三诺	Project: 120S-11&14IAP	
	Engineer: Lear	
Size: Custom	Title: <POWER SEQUENCE>	Rev: V01
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SHEET NO.	SHEET NAME
1	BLOCK DIAGRAM
2	TABLE OF CONTENTS
3	POWER SEQUENCE
4	APL SOC-LPDDR4 CH0
5	APL SOC-LPDDR4 CH1
6	APL SOC-DISPLAY
7	APL SOC-PCIE&USB
8	APL SOC-EMMC,SPI,LPC
9	APL SOC- I2C&HDA
10	APL SOC-PMU,CRYSTAL,RTC
11	APL SOC-MISC
12	APL SOC-POWER
13	APL SOC-GND
14	APL SOC-(DECAP)
15	APL SOC- (BOOT STRAP)
16	MEM_LPDDR4 CH0 1 OF 2
17	MEM_LPDDR4 CH0 2 OF 2
18	MEM_LPDDR4 CH1 1 OF 2
19	MEM_LPDDR4 CH1 2 OF 2
20	NC
21	NC
22	MEM_LPDDR4 DECAPS
23	SYSTEM_FLASH
24	EMMC
25	NC
26	SENSORS
27	NC
28	SSD-M.2_HDD-CONN
29	AUDIO CODEC
30	AUDIO_HEADSET AND SPEAKERS
31	GAUGE&BATTERY CONN
32	DC JACK
33	NC
34	NC
35	WIFI/BT M.2 CONN
36	TYPE C MUX&CONNECTOR
37	HDMI LEVEL SHIFTER
38	HDMI CONN
39	DISPLAY
40	+V5P0A ,+V3P3SX,+V5P0SX

SHEET NO.	SHEET NAME
41	NC
42	NC
43	NC
44	NC
45	EC-1
46	EC-2 (LED, BUTTON)
47	EC-3 (KEYBOARD,TP CONN)
48	NC
49	USB CHANGER,USB3.0 CONN
50	IO&DEBUG CONN
51	MISC
52	NC
53	SCREW
54	BATTERY CHARGER
55	PWR +V3P3A AND +5CP
56	PWR-DDR
57	PWR-NC
58	PWR-+V1P05S
59	PWR-+V1P24A
60	PWR-+V1P8A
61	VCGI AND VNN_1
62	VCGI AND VNN_2
63	PWR BLOCK DIAGRAM

BPAGE DRAWING

apl_ff.s
Fri May 27 06:47:10 2016

3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: TABLE OF CONTENTS	Rev: V01
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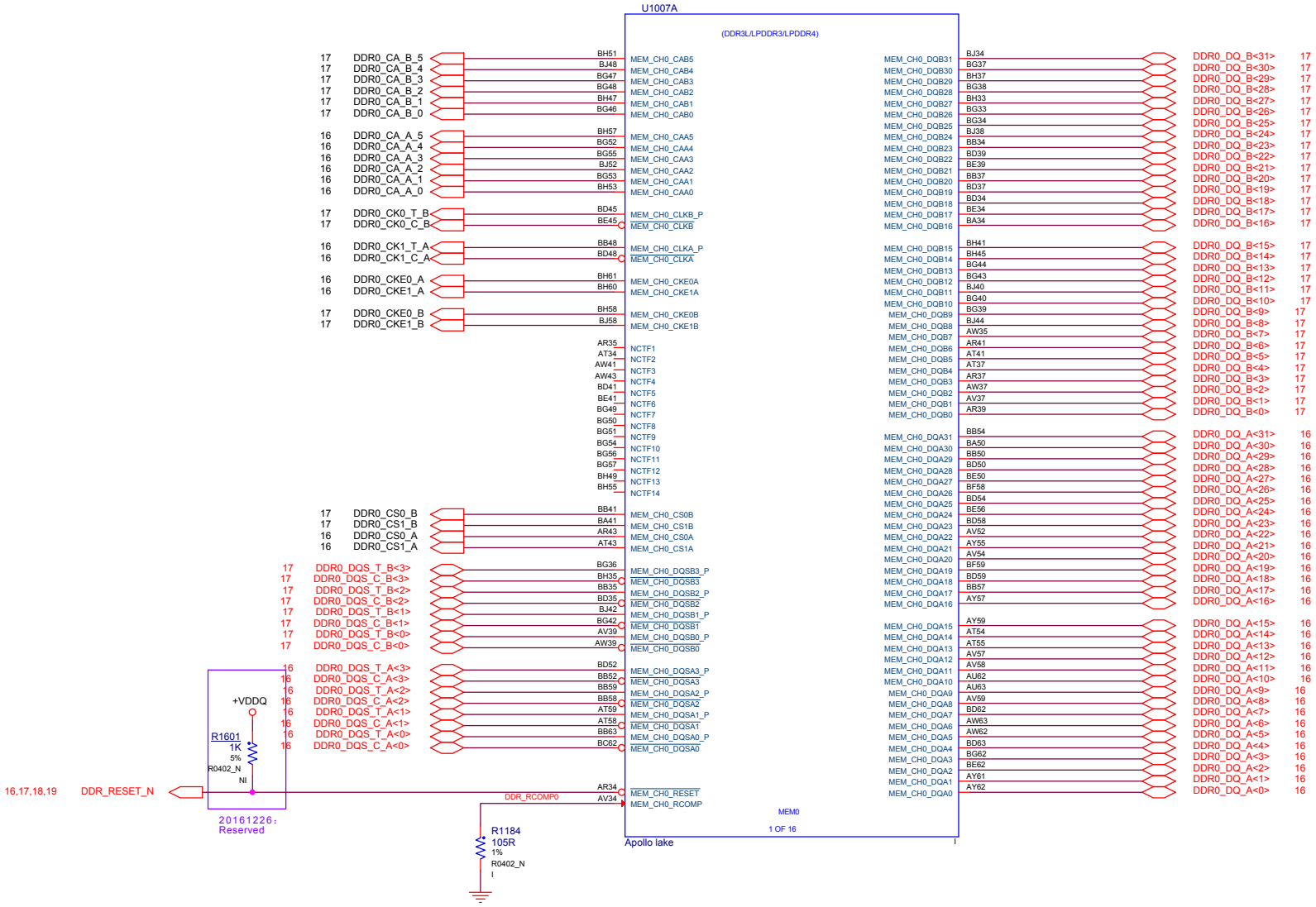

INTERNAL ONLY

BPAGE DRAWING

apl_ff.UN$20.205
Fri May 27 06:47:34 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title:	<APL SOC-LPDDR4 CH0>
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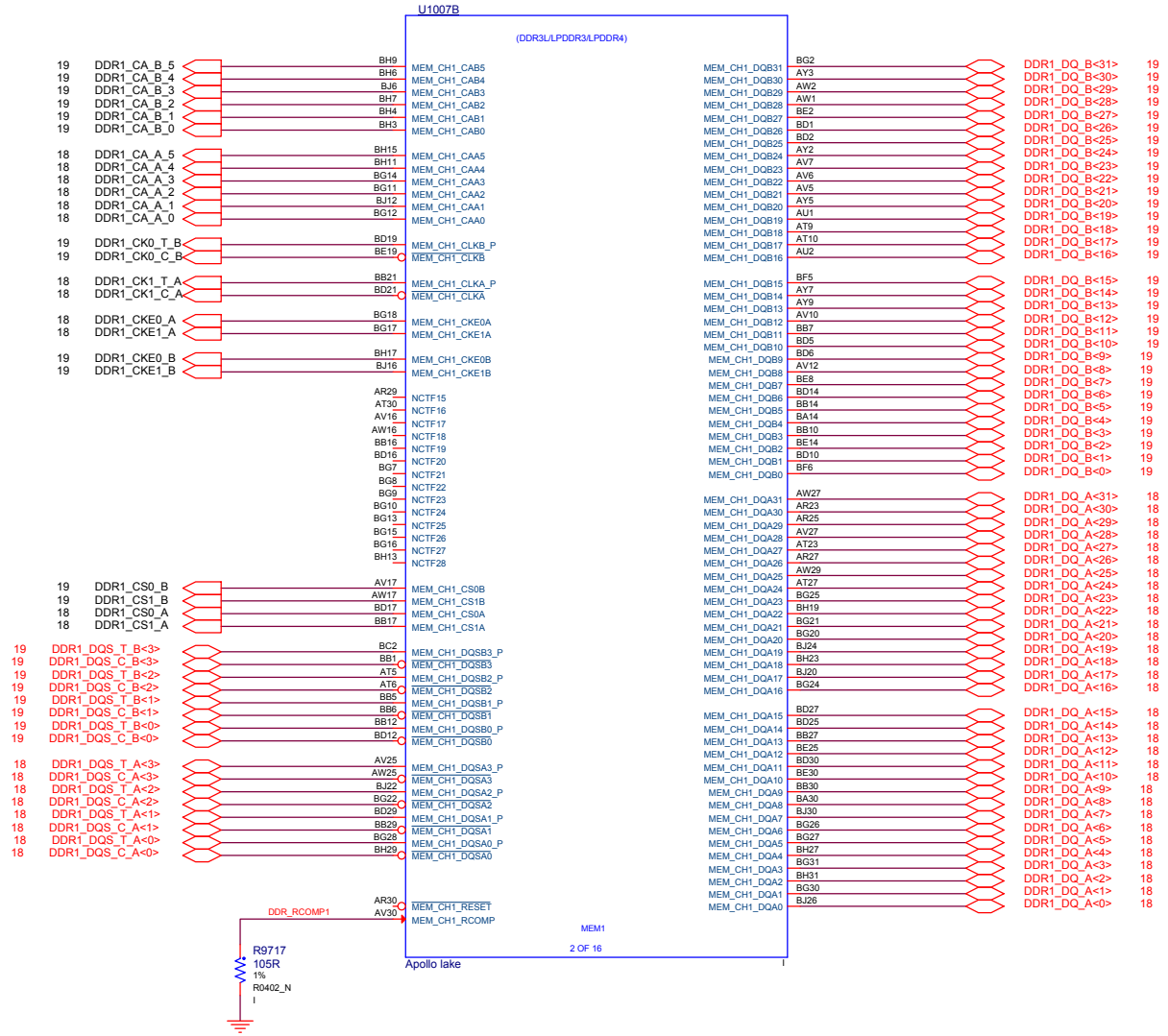
SOC: LPDDR4 CH1



BPAGE DRAWING

apl_ifl.8A
Fri May 27 06:47:12 2016

3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: SOC-LDDR4 CH1	Rev: V01
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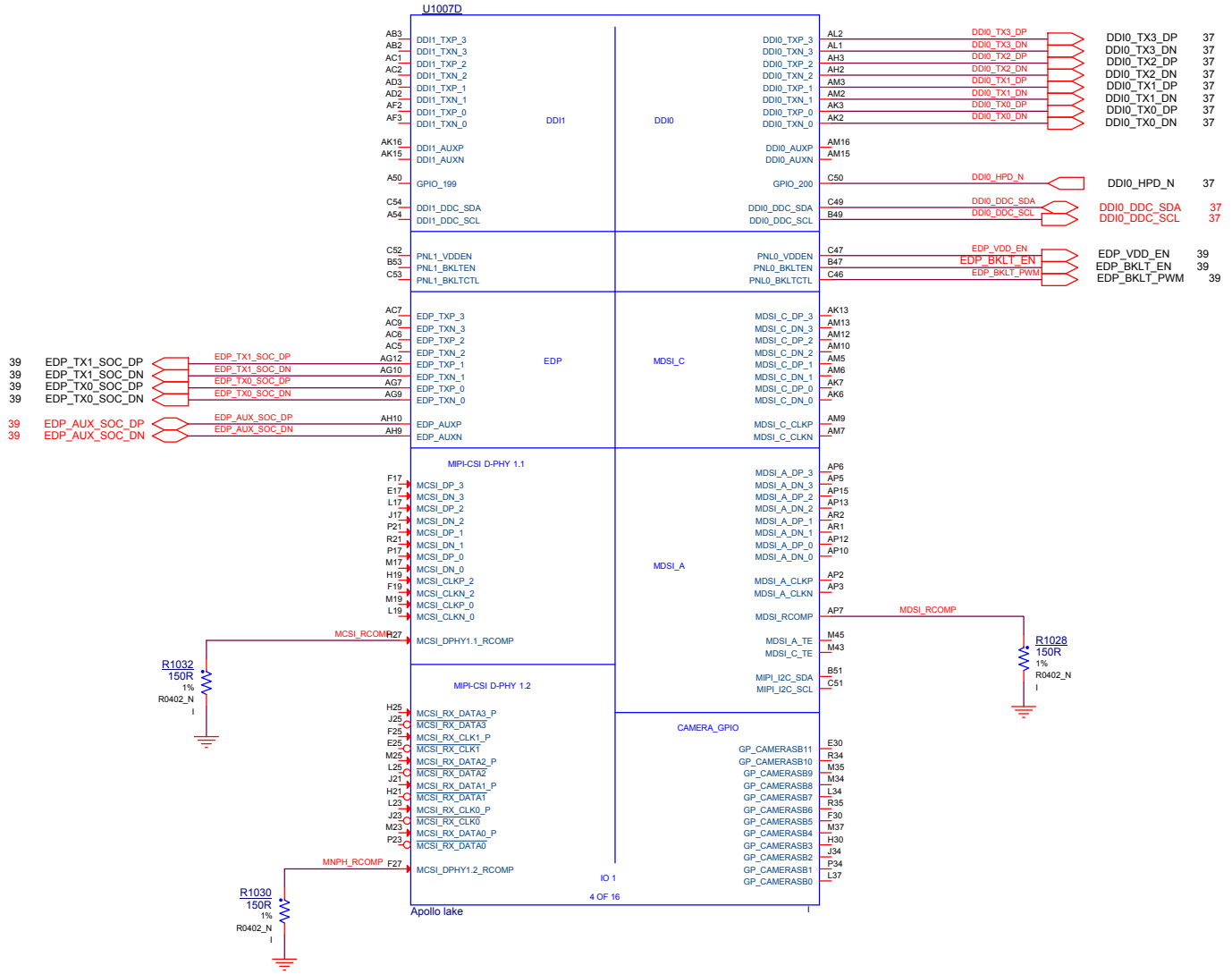

BPAGE DRAWING

apl_ff.GND
Fri May 27 06:47:12 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: SOC-DISPLAY	Rev: V01
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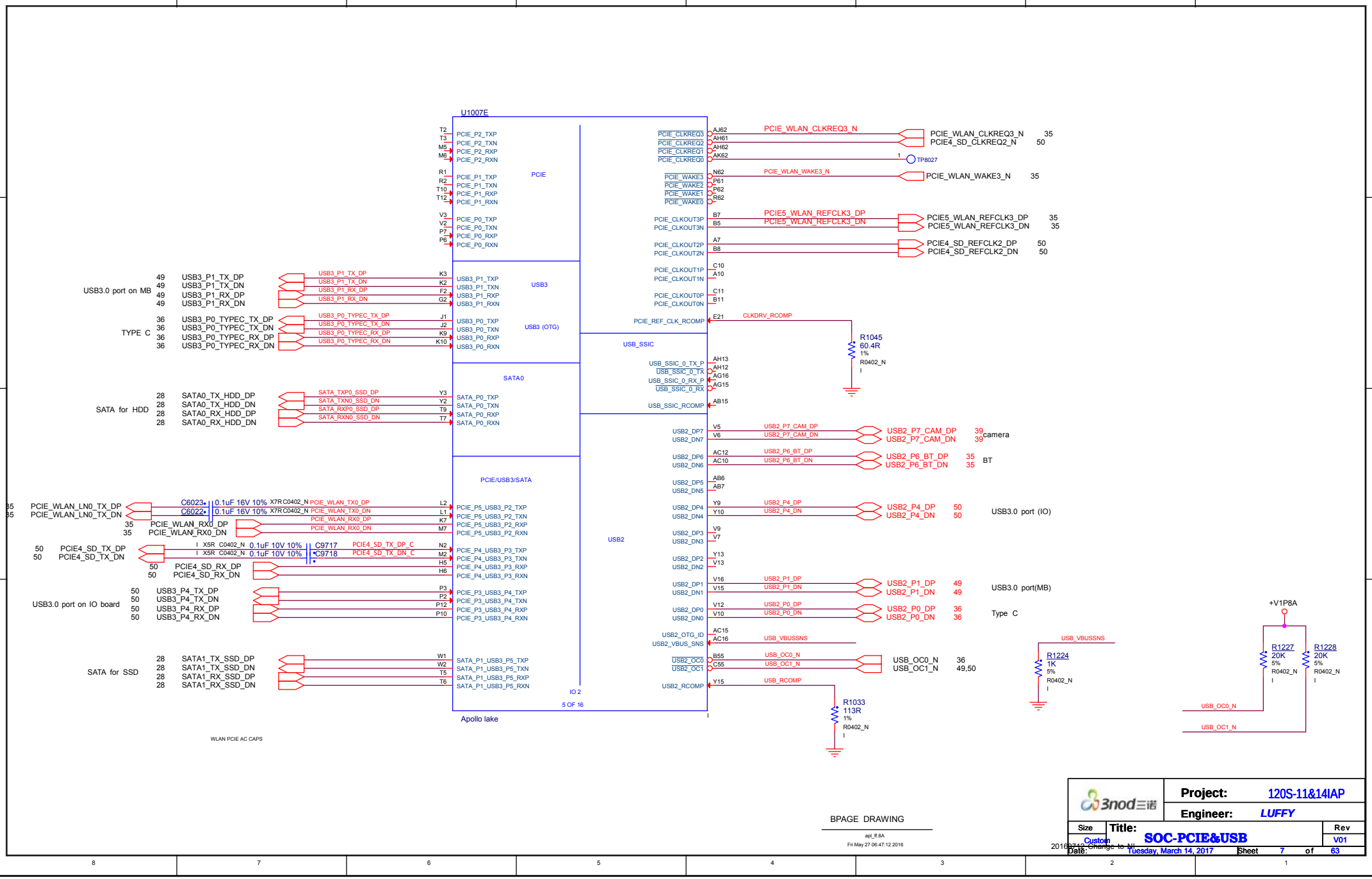

BPAGE DRAWING

apl_ifl.8A
Fri May 27 06:47:12 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: SOC-PCIE&USB	Rev: V01
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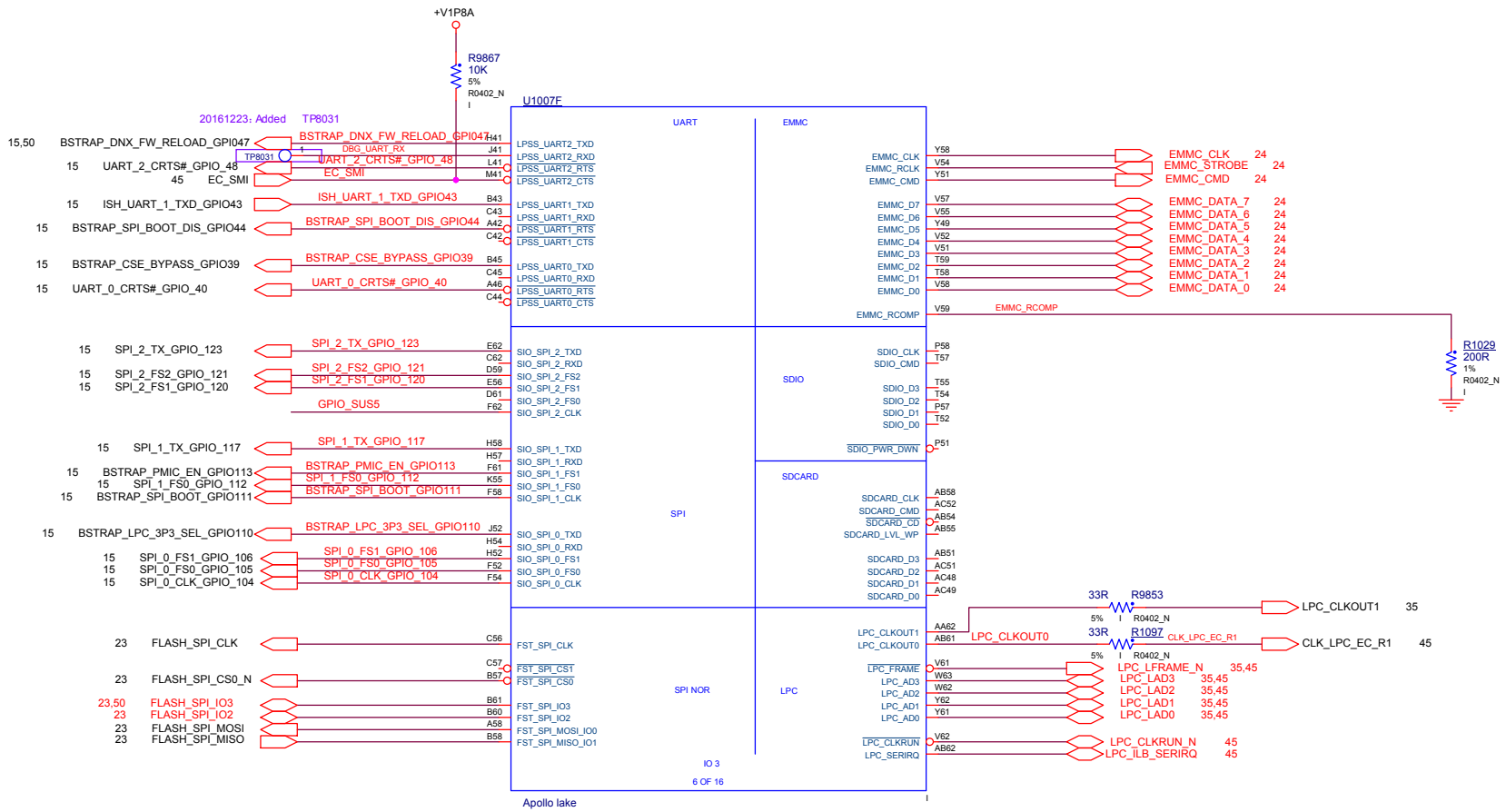
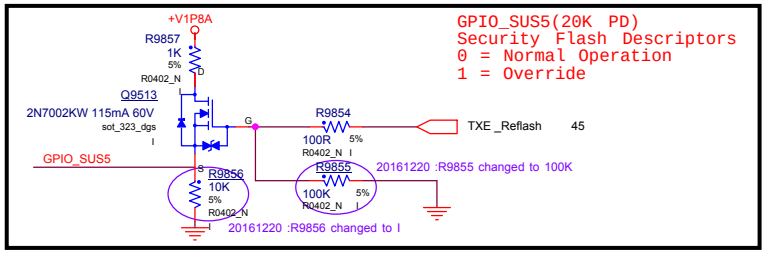
2016071?_change to NI





20161220 :Modified

CONN TBD

R1199 - EMMC BOOT STRAP

BPAGE DRAWING

apl_lf.GND
Fri May 27 06:47:12 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title:	SOC-EMMC,SPI,LPC
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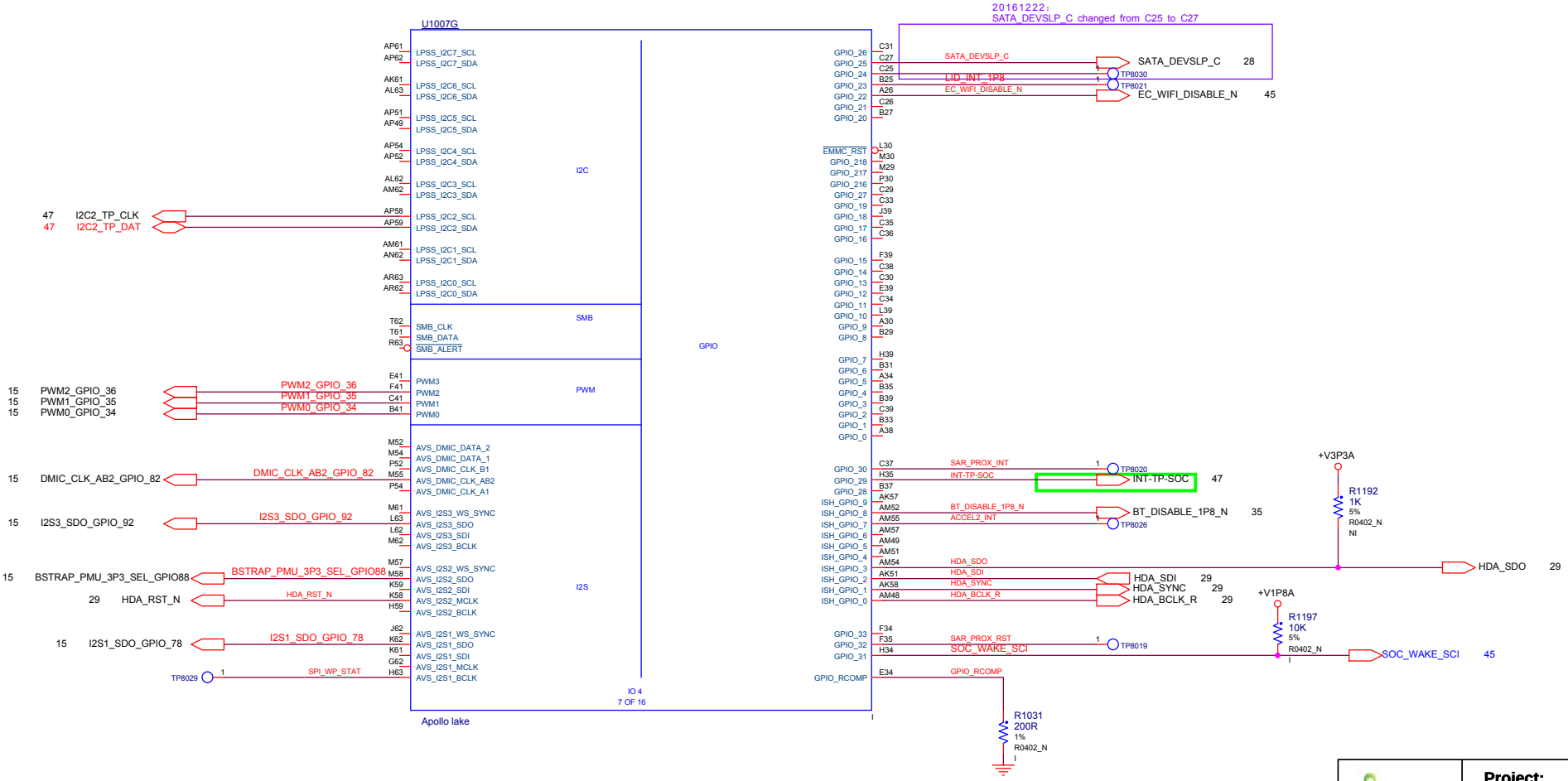

BPAGE DRAWING

apl_ff_UN885.8
Fri May 27 06:47:14 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: SOC- I2C&HDA	Rev: V01
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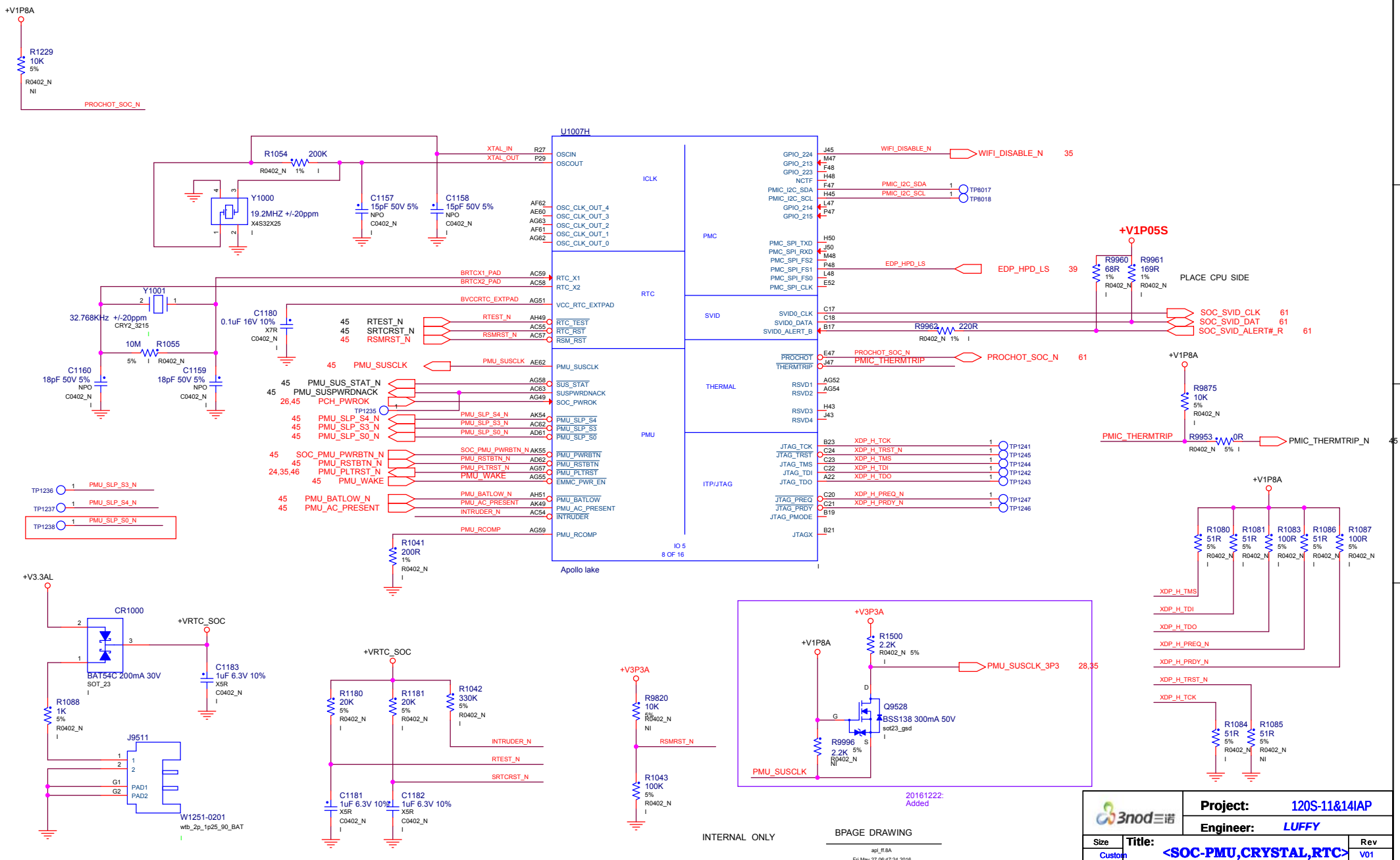
U1007H
Apollo lake
+V1P8A
R1229 10K 5% R0402_N NI
PROCHOT_SOC_N
R1054 200K R0402_N 1%
Y1000 19.2MHZ +/-20ppm X4S32X25
C1157 15pF 50V 5% NPO C0402_N
C1158 15pF 50V 5% NPO C0402_N
XTAL_IN
XTAL_OUT
Y1001 32.768KHz +/-20ppm CRY2_3215
C1180 0.1uF 16V 10% X7R C0402_N
10M R1055 5% R0402_N
C1160 18pF 50V 5% NPO C0402_N
C1159 18pF 50V 5% NPO C0402_N
BRTCX1_PAD
BRTCX2_PAD
BVCCRTC_EXTPAD
RTEST_N
SRTCRST_N
RSMRST_N
PMU_SUSCLK
PMU_SUS_STAT_N
PMU_SUSPWRDNACK
PCH_PWROK
PMU_SLP_S4_N
PMU_SLP_S3_N
PMU_SLP_S0_N
SOC_PMU_PWRBTN_N
PMU_RSTBTN_N
PMU_PLTRST_N
PMU_WAKE
PMU_BATLOW_N
PMU_AC_PRESENT
INTRUDER_N
PMU_RCOMP
R1041 200R 1% R0402_N
TP1236 PMU_SLP_S3_N
TP1237 PMU_SLP_S4_N
TP1238 PMU_SLP_S0_N
ICLK
RTC
PMC
SVID
THERMAL
PMU
ITP/JTAG
IO 5
8 OF 16
WIFI_DISABLE_N
PMIC_I2C_SDA
PMIC_I2C_SCL
TP8017
TP8018
EDP_HPD_LS
+V1P05S
R9960 68R 1% R0402_N
R9961 169R 1% R0402_N
PLACE CPU SIDE
SOC_SVID_CLK
SOC_SVID_DAT
SOC_SVID_ALERT#_R
R9962 220R R0402_N 1%
PROCHOT_SOC_N
PMIC_THERMTRIP
R9875 10K 5% R0402_N
R9953 0R R0402_N 5%
PMIC_THERMTRIP_N
JTAG_TCK
JTAG_TRST
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_PREQ
JTAG_PRDY
JTAG_PMODE
JTAGX
XDP_H_TCK
XDP_H_TRST_N
XDP_H_TMS
XDP_H_TDI
XDP_H_TDO
XDP_H_PREQ_N
XDP_H_PRDY_N
TP1241
TP1245
TP1244
TP1242
TP1243
TP1247
TP1246
R1080 51R 5% R0402_N
R1081 51R 5% R0402_N
R1083 100R 5% R0402_N
R1086 51R 5% R0402_N
R1087 100R 5% R0402_N
R1084 51R 5% R0402_N
R1085 51R 5% R0402_N NI
+V3.3AL
CR1000 BAT54C 200mA 30V SOT_23
+VRTC_SOC
C1183 1uF 6.3V 10% X5R C0402_N
R1088 1K 5% R0402_N
J9511
PAD1
PAD2
W1251-0201 wtb_2p_1p25_90_BAT
R1180 20K 5% R0402_N
R1181 20K 5% R0402_N
R1042 330K 5% R0402_N
C1181 1uF 6.3V 10% X5R C0402_N
C1182 1uF 6.3V 10% X5R C0402_N
+V3P3A
R9820 10K 5% R0402_N NI
R1043 100K 5% R0402_N
RSMRST_N
R1500 2.2K R0402_N 5%
PMU_SUSCLK_3P3
Q9528 BSS138 300mA 50V sot23_gsd
R9996 2.2K 5% R0402_N NI
20161222: Added
INTERNAL ONLY
BPAGE DRAWING
apl_ff.8A
Fri May 27 06:47:24 2016
Project: 120S-11&14IAP
Engineer: LUFFY
Size Custom
Title: <SOC-PMU,CRYSTAL,RTC>
Rev V01
Date: Tuesday, March 14, 2017
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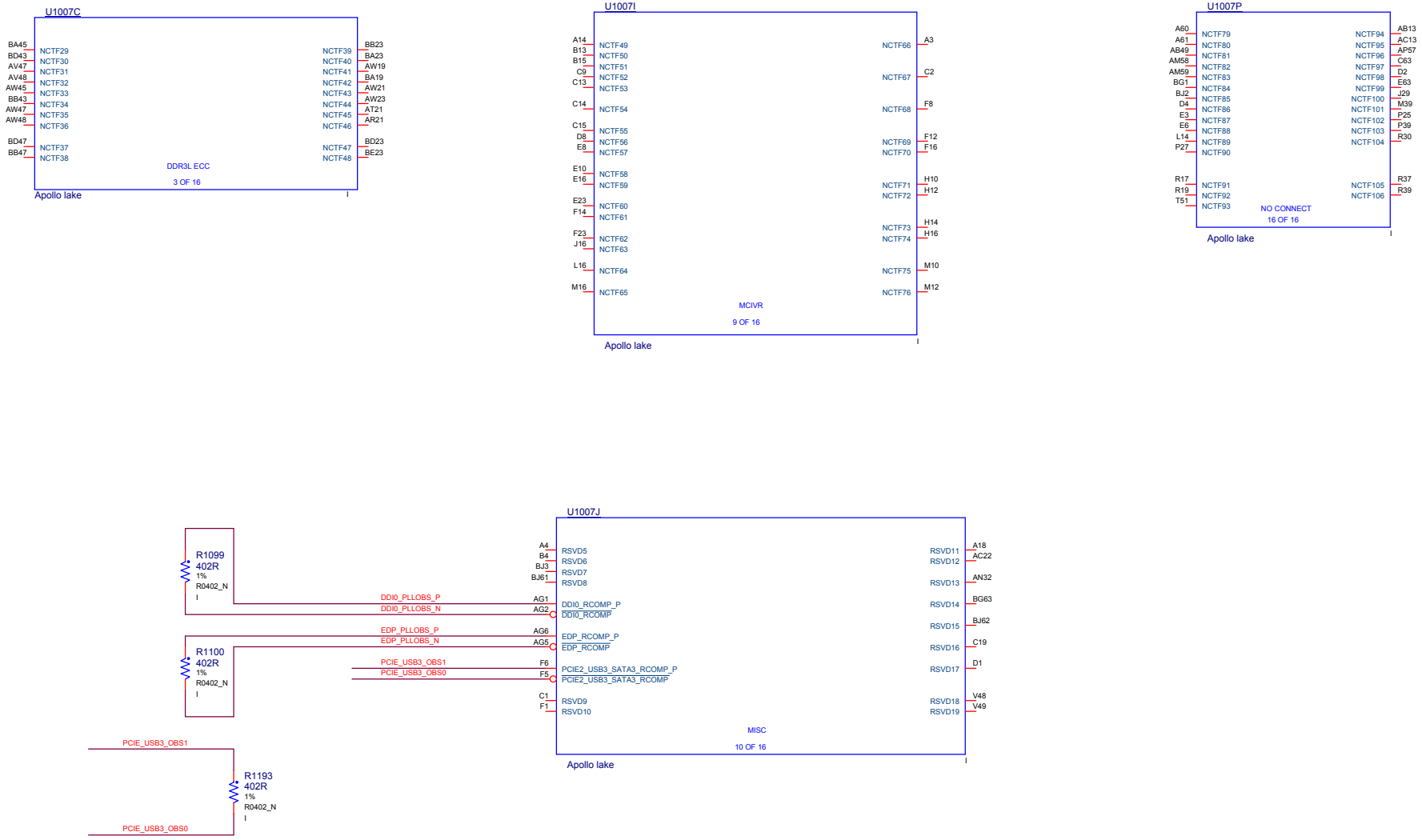

INTERNAL ONLY

BPAGE DRAWING

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Fri May 27 06:47:24 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: <SOC-MISC>	Rev: V01
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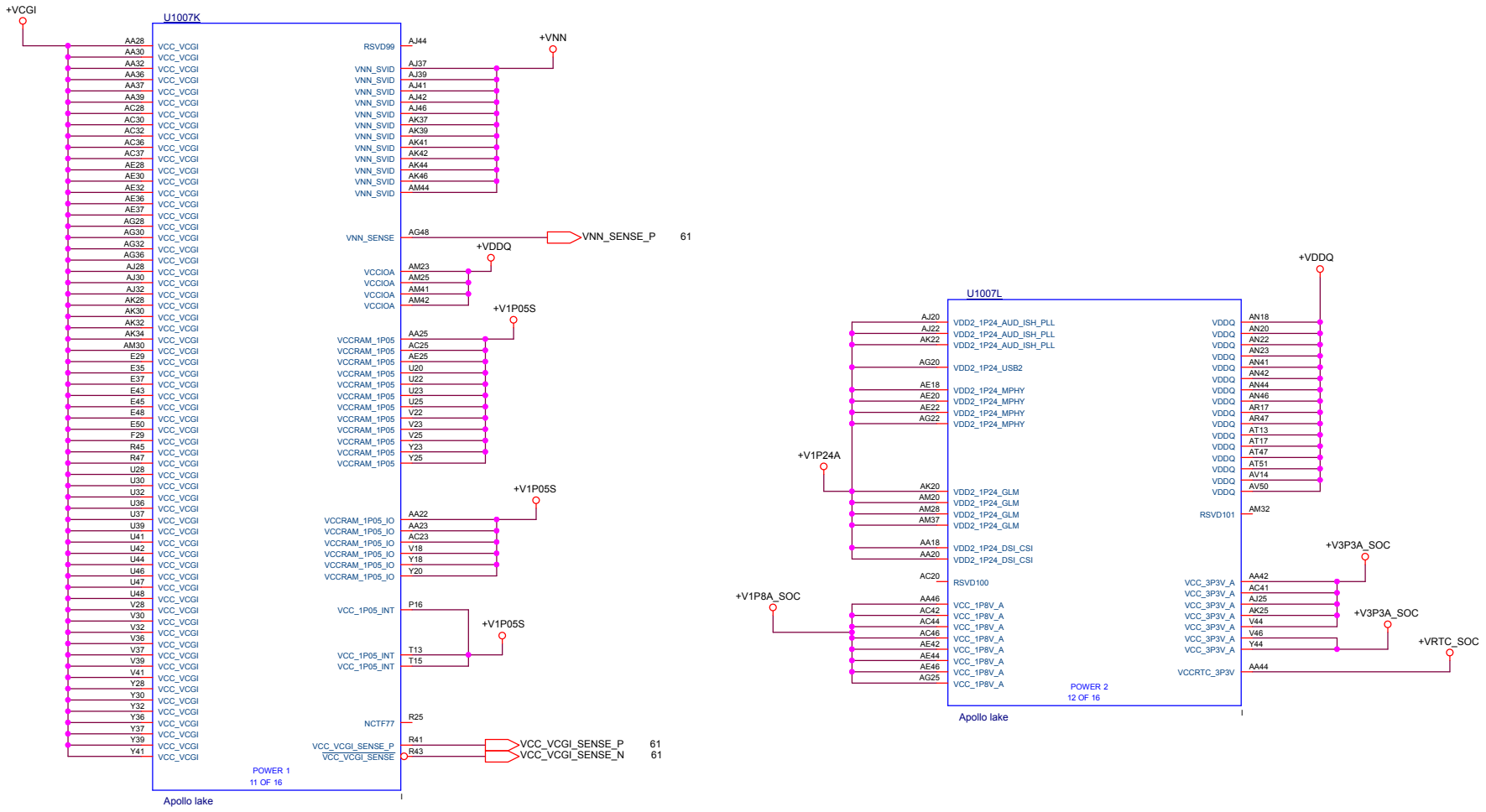
SOC: POWER



BPAGE DRAWING

apl_ff.+V1P0.9
Fri May 27 06:47:14 2016

3nod三诺	Project:	120S-11&14IAP	
	Engineer:	LUFFY	
Size: Custom	Title:	SOC-POWER	Rev: V01
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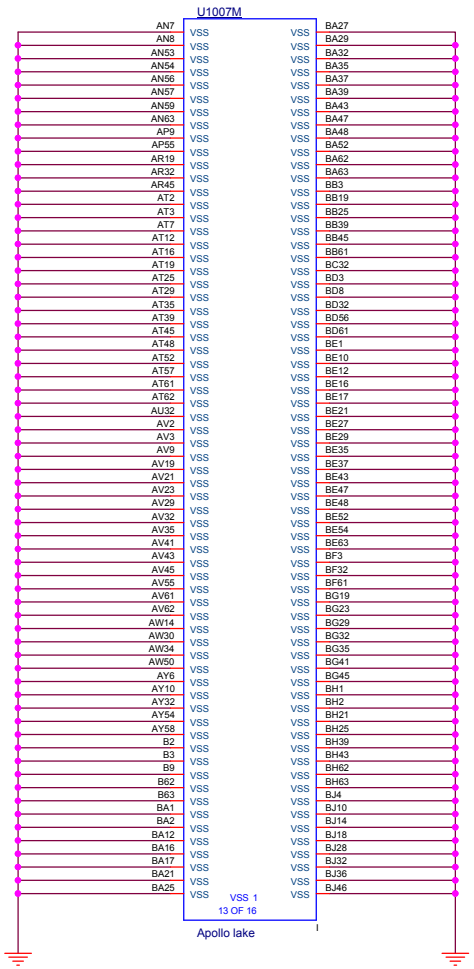
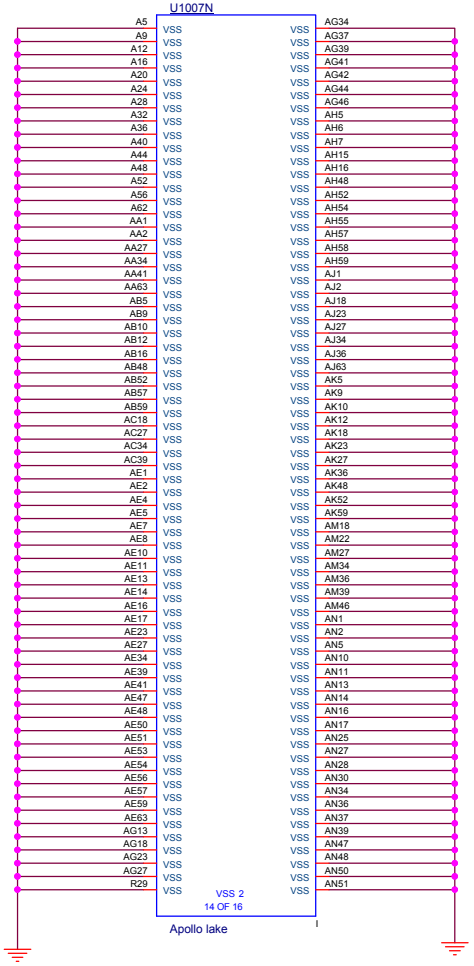
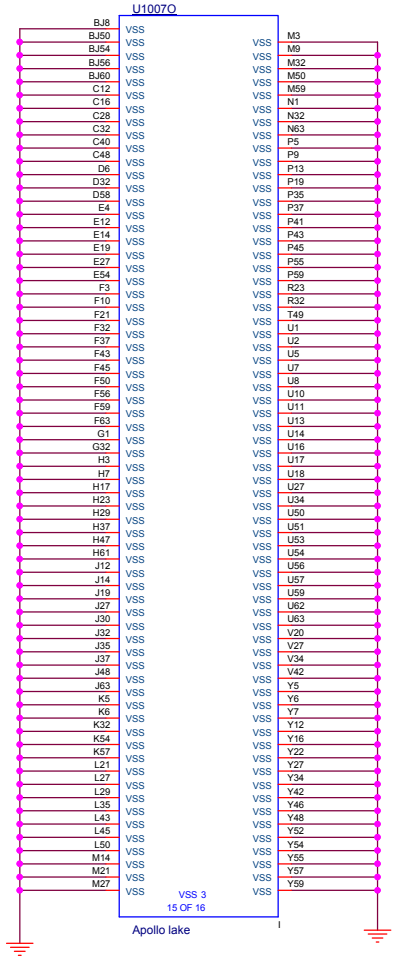
SOC: GND







BPAGE DRAWING

apl_ff.GND
Fri May 27 06:47:14 2016

3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: SOC-GND	Rev: V01
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SOC: DECAPS

CAD NOTE:
PLACE IN BETWEEN SOC AND DRAM

+V1P8A_SOC — +V1P8A
NOBOM
JUMP_43X39
JUMP-SH1110

+V3P3A_SOC — +V3P3A
NOBOM
JUMP_43X39
JUMP-SH1111

+VDDQ

C1073 22uF 6.3V 20% X5R C0603_N
C1081 22uF 6.3V 20% X5R C0603_N
C1088 22uF 6.3V 20% X5R C0603_N
C1093 22uF 6.3V 20% X5R C0603_N
C1071 22uF 6.3V 20% X5R C0603_N
C1075 22uF 6.3V 20% X5R C0603_N
C1076 22uF 6.3V 20% X5R C0603_N
C1078 22uF 6.3V 20% X5R C0603_N

20161223"
Changed the footprint to 0603

+V1P8A_SOC
BSC
C1132 1uF 6.3V 10% X5R C0402_N
C1135 1uF 6.3V 10% X5R C0402_N
C1138 1uF 6.3V 10% X5R C0402_N
C1140 1uF 6.3V 10% X5R C0402_N
C1143 22uF 6.3V 20% X5R C0603_N

+V3P3A_SOC
BSC
C1144 1uF 6.3V 10% X5R C0402_N
C1145 1uF 6.3V 10% X5R C0402_N
C1146 1uF 6.3V 10% X5R C0402_N
C1215 1uF 6.3V 10% X5R C0402_N
C1147 22uF 6.3V 20% X5R C0603_N

+VDDQ
BSC
C1241 1uF 6.3V 10% X5R C0402_N
C1242 1uF 6.3V 10% X5R C0402_N

+V1P24A
BSC
C1108 1uF 6.3V 10% X5R C0402_N
C1110 1uF 6.3V 10% X5R C0402_N
C1112 1uF 6.3V 10% X5R C0402_N
C1116 1uF 6.3V 10% X5R C0402_N
C1119 1uF 6.3V 10% X5R C0402_N
C1123 1uF 6.3V 10% X5R C0402_N
C1127 1uF 6.3V 10% X5R C0402_N
C1131 1uF 6.3V 10% X5R C0402_N

C1109 1uF 6.3V 10% X5R C0402_N
C1111 1uF 6.3V 10% X5R C0402_N
C1113 1uF 6.3V 10% X5R C0402_N
C1118 1uF 6.3V 10% X5R C0402_N
C1126 22uF 6.3V 20% X5R C0603_N
C1130 22uF 6.3V 20% X5R C0603_N
C1134 22uF 6.3V 20% X5R C0603_N
C1137 22uF 6.3V 20% X5R C0603_N

+VNN
BSC
C1235 1uF 6.3V 10% X5R C0402_N
C1086 1uF 6.3V 10% X5R C0402_N
C1092 1uF 6.3V 10% X5R C0402_N
C1097 1uF 6.3V 10% X5R C0402_N

+VNN
C1114 1uF 6.3V 10% X5R C0402_N

C1236 22uF 6.3V 20% X5R C0603_N
C1087 22uF 6.3V 20% X5R C0603_N
C1082 22uF 6.3V 20% X5R C0603_N
C1083 22uF 6.3V 20% X5R C0603_N
C1094 22uF 6.3V 20% X5R C0603_N
C1098 22uF 6.3V 20% X5R C0603_N

+VRTC_SOC
C1142 1uF 6.3V 10% X5R C0402_N

CAD NOTE: C1142 PLACE CLOSE TO PIN AA44

+VCGI
BSC
C1067 1uF 6.3V 10% X5R C0402_N
C1069 1uF 6.3V 10% X5R C0402_N
C1074 1uF 6.3V 10% X5R C0402_N
C1079 1uF 6.3V 10% X5R C0402_N
C1085 1uF 6.3V 10% X5R C0402_N
C1091 1uF 6.3V 10% X5R C0402_N
C1096 1uF 6.3V 10% X5R C0402_N
C1100 1uF 6.3V 10% X5R C0402_N
C1102 1uF 6.3V 10% X5R C0402_N
C1104 1uF 6.3V 10% X5R C0402_N
C1105 1uF 6.3V 10% X5R C0402_N
C1214 1uF 6.3V 10% X5R C0402_N

C1068 22uF 6.3V 20% X5R C0603_N
MLCC
C1089 22uF 6.3V 20% X5R C0603_N
C1095 22uF 6.3V 20% X5R C0603_N
C1099 22uF 6.3V 20% X5R C0603_N
C1103 22uF 6.3V 20% X5R C0603_N

20170323 Deleted C1169

20170323 Deleted C1072,C1077,C1084

20170207 Changed to NI;
20170210 Deleted C1007/C1015

C1148 1uF 6.3V 10% X5R C0402_N
C1149 1uF 6.3V 10% X5R C0402_N

+V1P05S
C1117 1uF 6.3V 10% X5R C0402_N
C1121 1uF 6.3V 10% X5R C0402_N
C1125 1uF 6.3V 10% X5R C0402_N
C1129 1uF 6.3V 10% X5R C0402_N
C1133 22uF 6.3V 20% X5R C0603_N
C1136 22uF 6.3V 20% X5R C0603_N
C1139 22uF 6.3V 20% X5R C0603_N

BSC
C1115 1uF 6.3V 10% X5R C0402_N
C1120 1uF 6.3V 10% X5R C0402_N
C1124 1uF 6.3V 10% X5R C0402_N
C1128 1uF 6.3V 10% X5R C0402_N

BPAGE DRAWING
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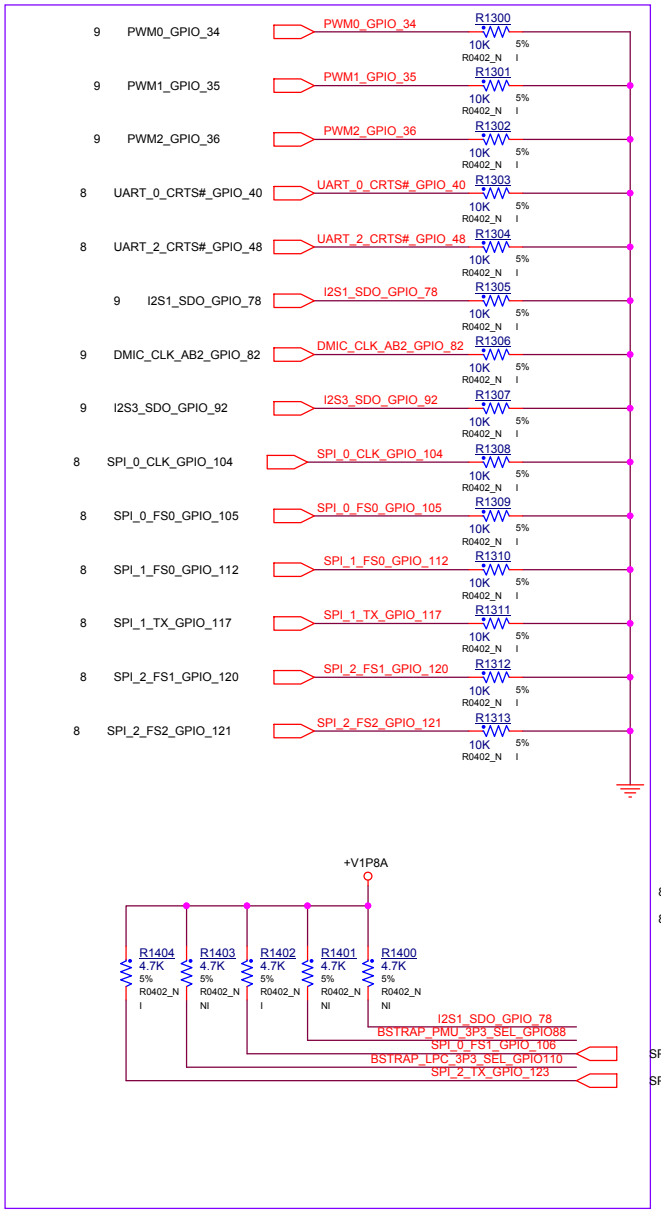
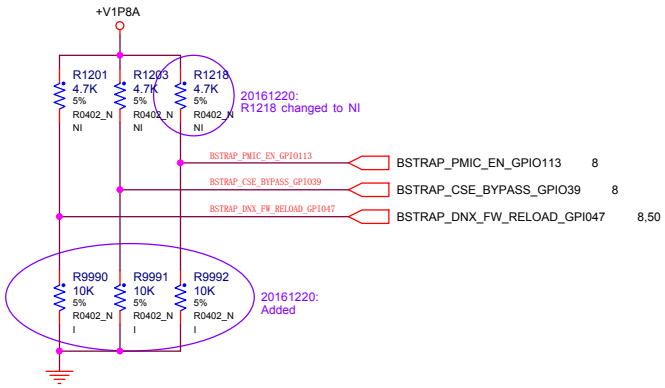
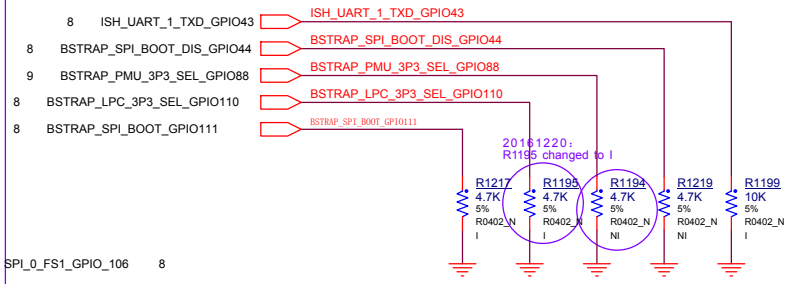
Fri May 27 06:47:16 2016

3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: SOC-(DECAP)	Rev: V01
Date: Thursday, March 23, 2017	Sheet 14 of 63	

SOC: 7 OF 12







BSTRAP_LPC_3P3_SEL: LPC 1V8/3V3 mode select(20K PU)
1=buffers set to 1V8 mode(default)
0=buffers set to 3v3 mode(default)

BXT-P GPIO	SOC Ball Name	BSTRAP	Default Internal PU/PD
GPIO34	PWM0	Delayed_vref_switch) 0= not delayed(Default) 1=delayed	PD
GPIO35	PWM1	Spare1 0= do not stall boot FSM(Default) 1=stall boot FSM	PD
GPIO36	PWM2	Spare2 0 =VDD2 IS 1.24V(Default) 1=VDD2 IS 1.35V	PD
GPIO39	LPASS_UART0_TXD	Eable CSE ROM bypass 0 = disable bypass (default) 1 = enable bypass	PD
GPIO40	RTC Clock Timer Bypass	RTC Clock Timer Bypass 0 =disable bypass (Default) 1 =enable bypass	PD
GPIO43	LPASS_UART1_TXD	Select eMMC boot source 0 =do now allow (Default) 1=allow	PU
GPIO44	LPASS_UART1_RTS_B	Select SPI boot source 0 =Disable 1=Enable(Default)	PU
GPIO47	LPASS_UART2_TXD	Force DNX FW Load 0 =Disable(Default) 1=Enable	PD
GPIO48	LPASS_UART2_RTS_B	LPC Boot strap 0 =Do not boot from LPC(Default) 1=Enable	PD
GPIO78	AVS_I2S1_SDO	SMBus 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode (default)	PU
GPIO82	AVS_M_CLK_AB2	WC_PRESENT 0=non-Whiskey Cove(Default) 1=Whiskey Cove is connected	PD
GPIO88	AVS_I2S2_SD0	PMU (Power Management Unit) 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode (default)	PU
GPIO92	AVS_I2S3_SD0	SMBus No Re-Boot 0=Dsiable(Default) 1=Enable	PD
GPIO104	GP_SSP_0_CLK	(HVM Tester)XTAL startup 0=Dsiable(Default) 1=Enable	PD
GPIO105	GP_SSP_0_FS0	(HVM Tester)XTAL startup 0=Dsiable(Default) 1=Enable	PU
GPIO106	GP_SSP_0_FS1	Halts early boot for debug 0=Enable 1=Disable	PU
GPIO110	GP_SSP_0_TXD	LPC 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode (default)	PU
GPIO111	GP_SSP_1_CLK	SPI Boot BIOS strap 0=boot from SPI(Debug) 1=Do not boot from SPI (default)	PU
GPIO112	GP_SSP_1_FS0	Enable metal password auth 0=Disable 1=Enable	PD
GPIO113	GP_SSP_1_FS1	SVID diable 0=Enable SVID(Default) 1=Disbale SVID	PU
GPIO117	GP_SSP_1_TXD	Stall BOot FSM for debut 0=Do not stall boot FSM(Default) 1=stall boot FSM	PD
GPIO118	GP_SSP_2_CLK	Flash Descriptpr Override Pin-Strao status 0=Disable(Default) 1=Enable	PD
GPIO120	GP_SSP_2_FS1	Top swap pverride 0=Disable(Default) 1=Enable	PD
GPIO121	GP_SSP_2_FS2	Plled LOW when RSM_RST_N deasserts	PD
GPIO123	GP_SSP_2_TXD	Pulled HIGH when RSM_RST_N de-asserts	PU

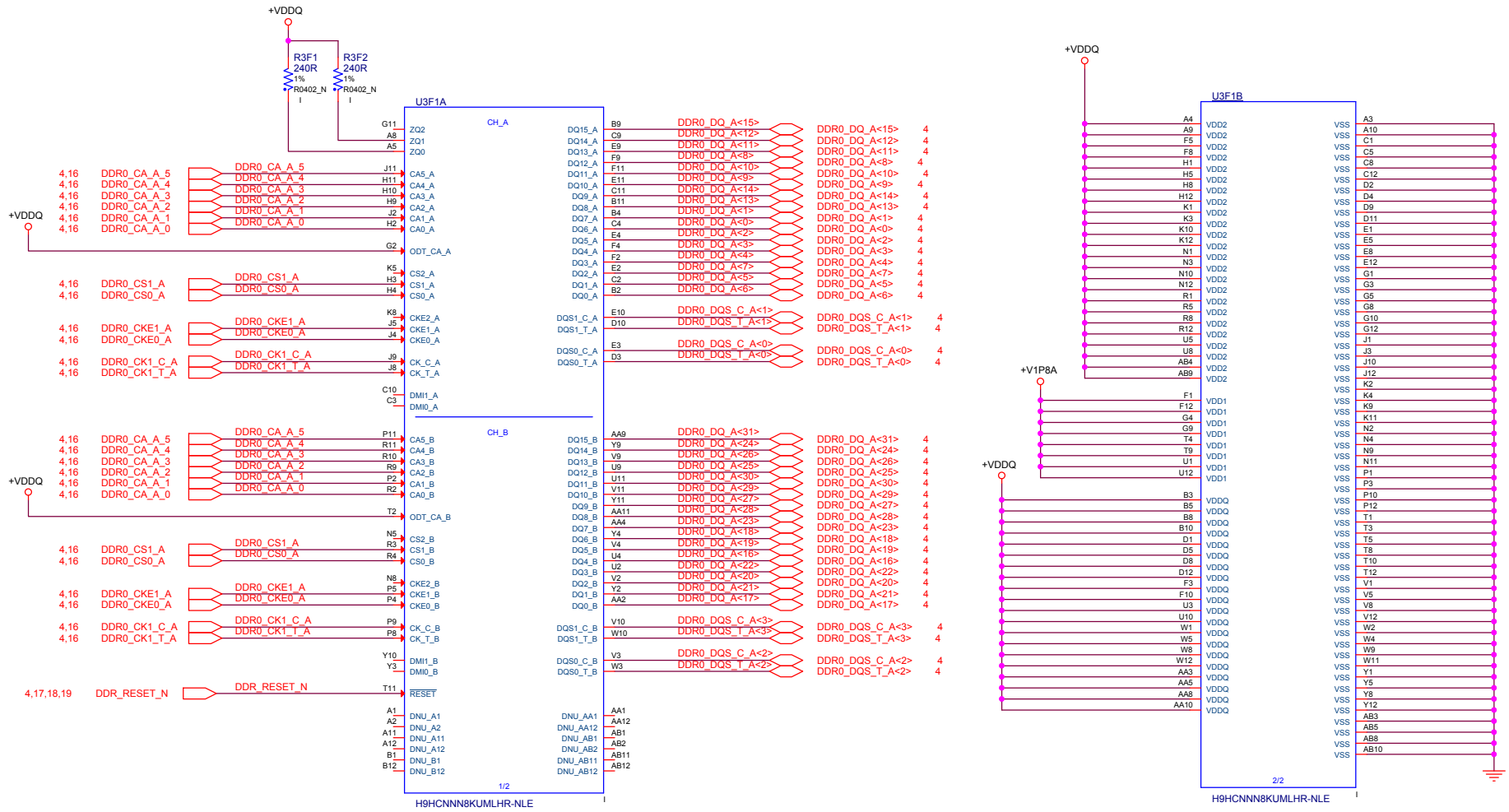
20161220:
Added

BPAGE DRAWING

apl_lf.GND
Fri May 27 06:47:16 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: SOC- (BOOT STRAP)	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 15 of 63	

CHANNEL 0 - MEMORY1/2

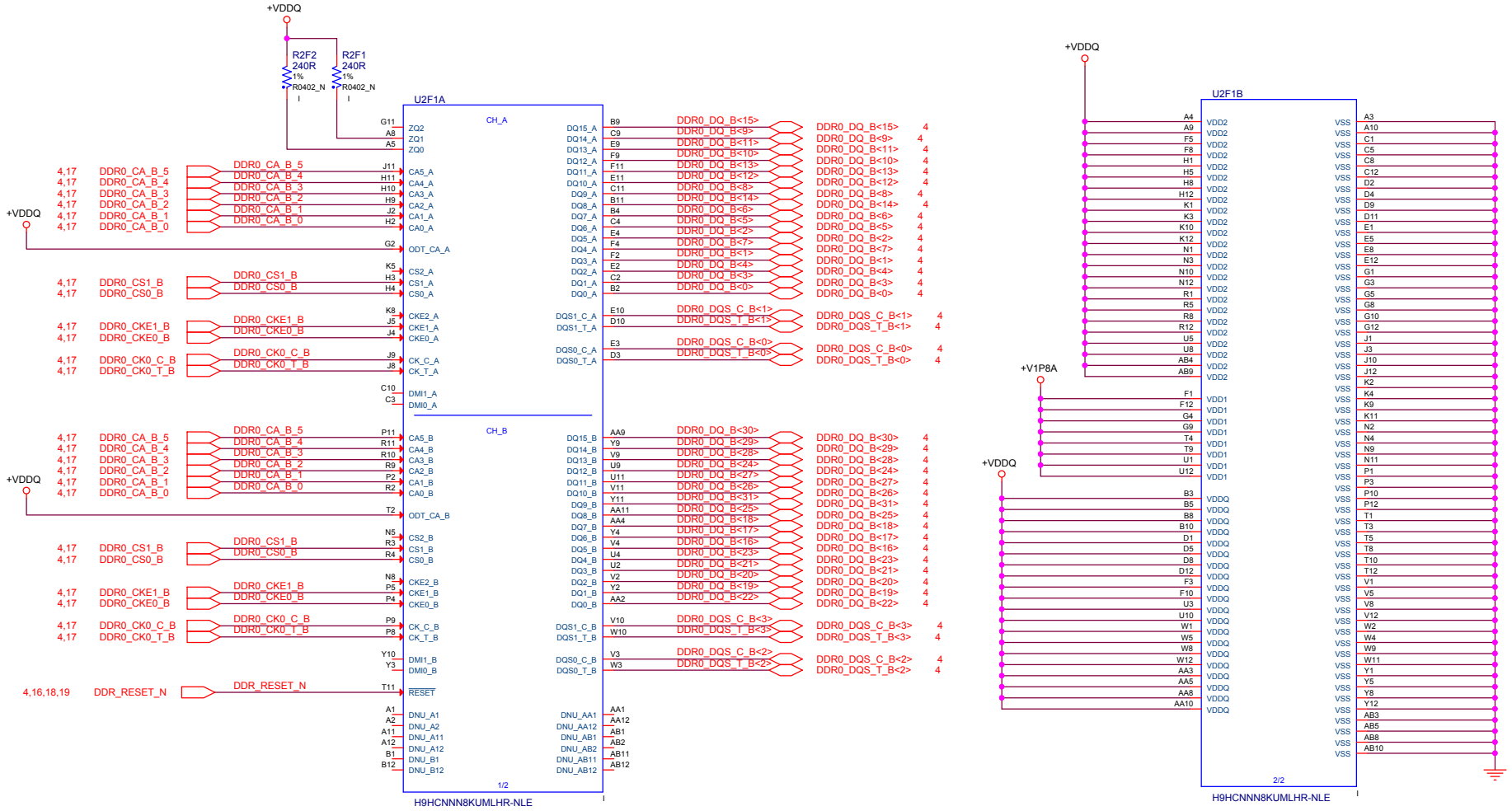


BPAGE DRAWING

apl_lf.GND
Fri May 27 06:47:16 2016

3nod三诺	Project:	120S-11&14IAP	
	Engineer:	LUFFY	
Size: Custom	Title:	MEM_LPDDR4 CH0-1 of 2	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 16 of 63		

CHANNEL 0 - MEMORY2/2

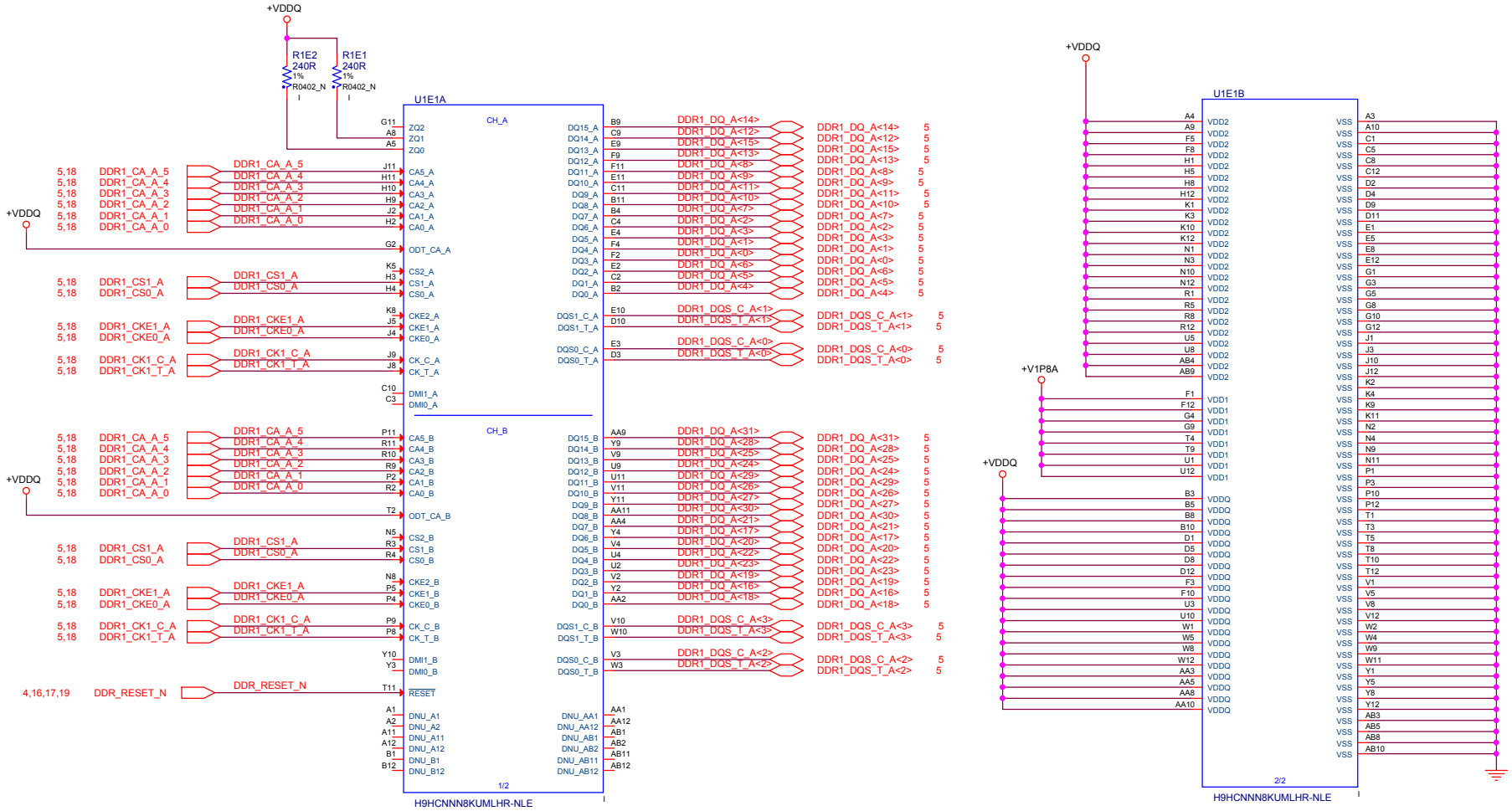


BPAGE DRAWING

apl_ff.GND
Fri May 27 06:47:16 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title:	MEM_LPDDR4 CH0-2 of 2
		Rev: V01
Date: Tuesday, March 14, 2017	Sheet 17 of 63	

CHANNEL 1 - MEMORY1/2

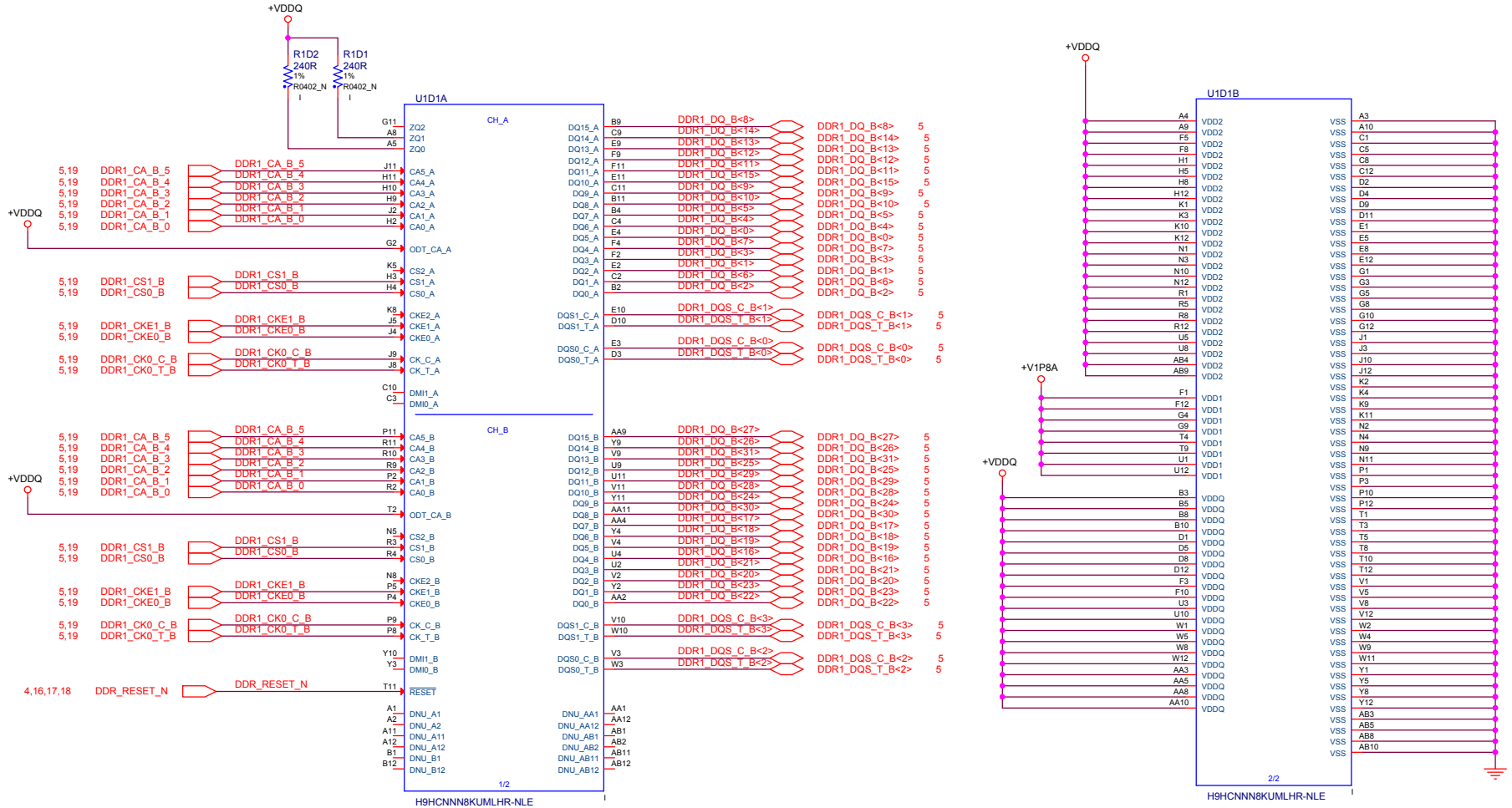


BPAGE DRAWING

apl_ff.GND
Fri May 27 06:47:18 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title:	MEM_LPDDR4 CH1-1 of 2
		Rev: V01
Date: Tuesday, March 14, 2017	Sheet 18 of 63	

CHANNEL 1 - MEMORY2/2



BPAGE DRAWING

apl_ff.GND
Fri May 27 06:47:18 2016

3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: MEM_LPDDR4 CH1-2of 2	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 19 of 63	

BPAGE DRAWING

apl_ff.+V1P8.18
Fri May 27 06:47:18 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: NC	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 20 of 63	

BPAGE DRAWING

apl_ff.+V1P8.18
Fri May 27 06:47:18 2016

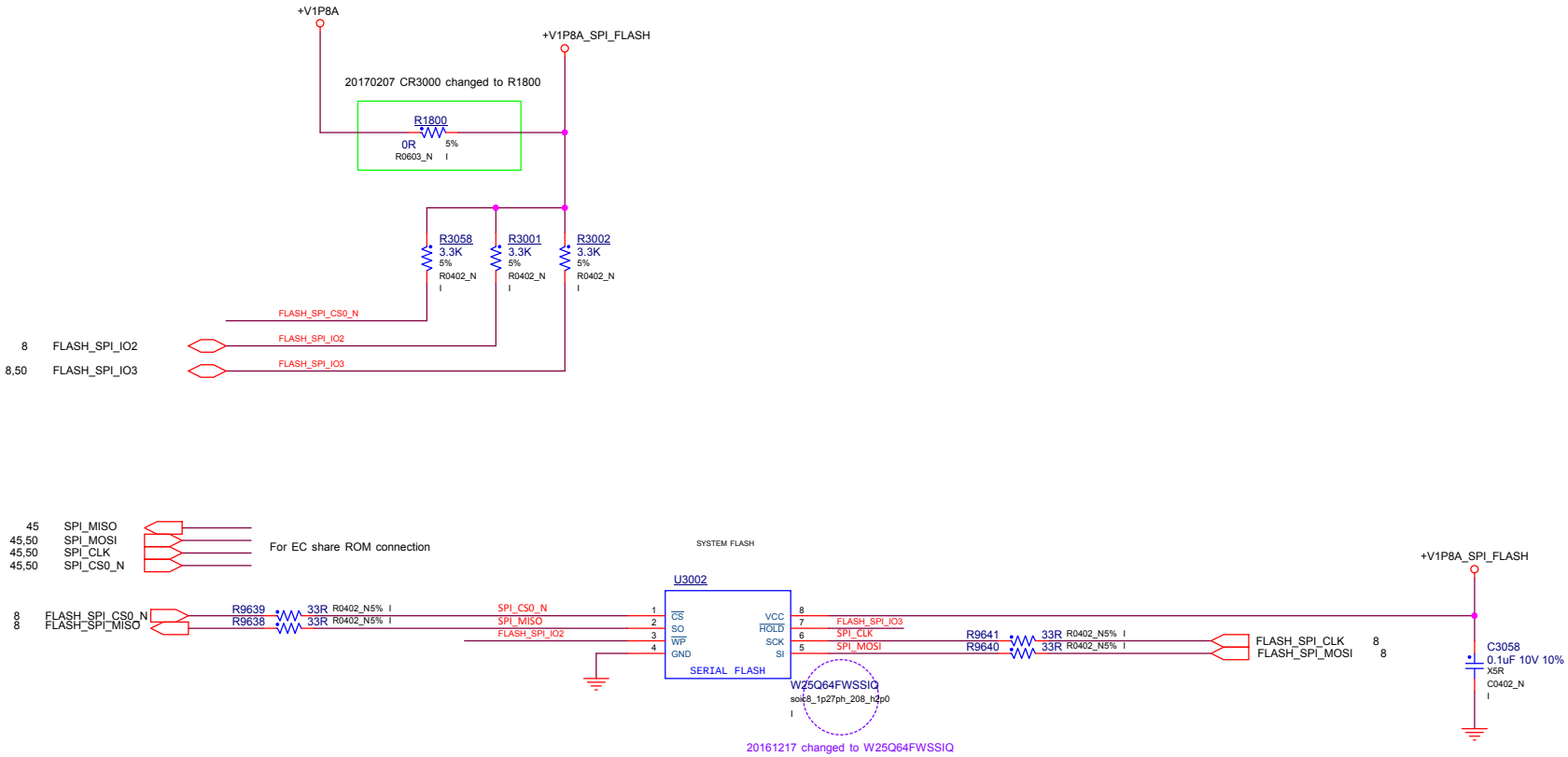
3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: NC	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 21 of 63	

BPAGE DRAWING

apl_ff.8A

Fri May 27 06:47:18 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: MEM_LPDDR4-DECAPS	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 22 of 63	

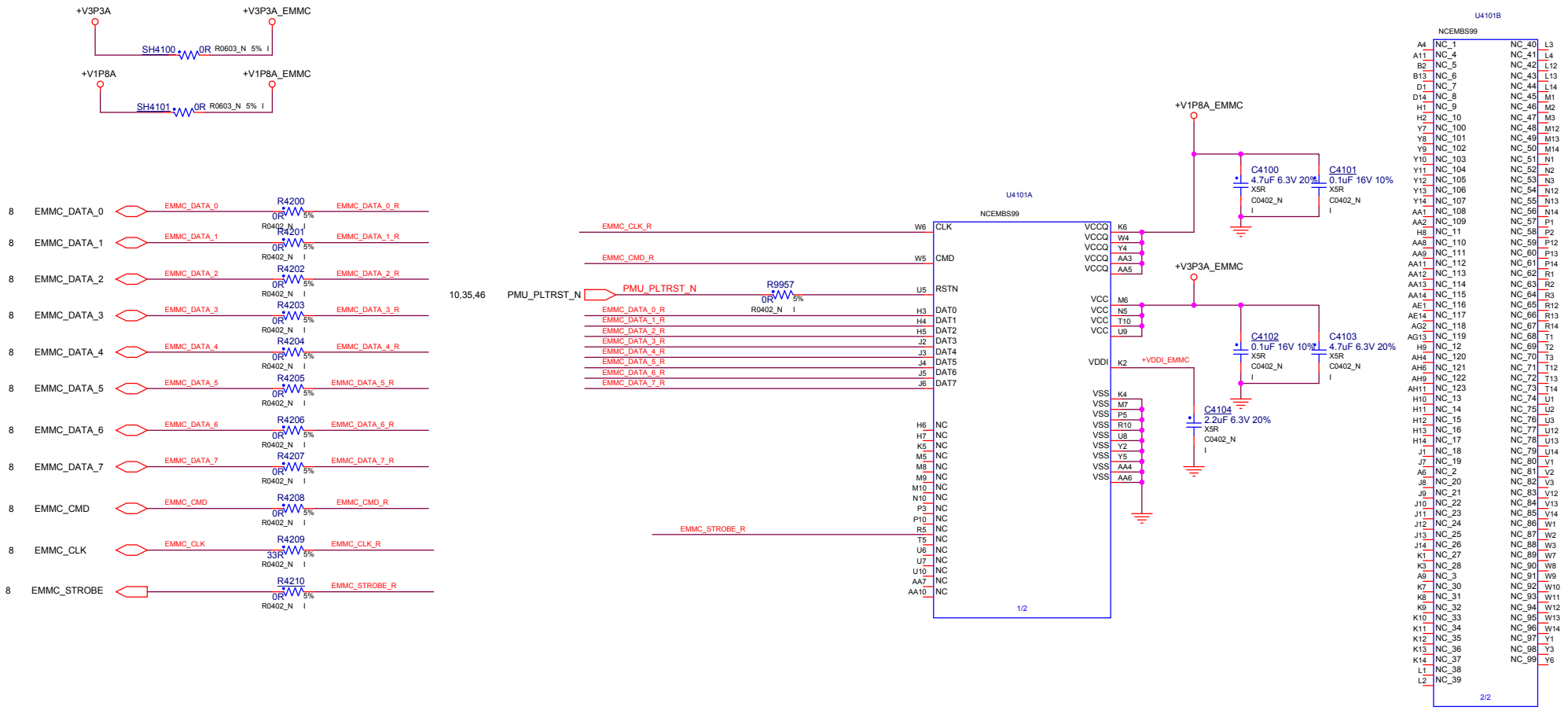


INTERNAL ONLY

BPAGE DRAWING

apl_ff.GND
Fri May 27 06:47:20 2016

3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: <SYSTEM_FLASH>	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 23 of 63	



INTERNAL ONLY

BPAGE DRAWING

apl_ff.GND
Fri May 27 06:47:20 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: <EMMC>	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 24 of 63	

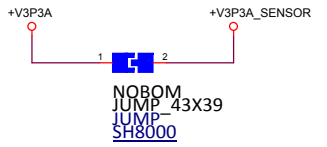
INTERNAL ONLY

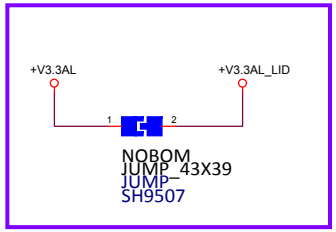
BPAGE DRAWING

apl_ff.s
Fri May 27 06:47:20 2016

3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: <NC>	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 25 of 63	

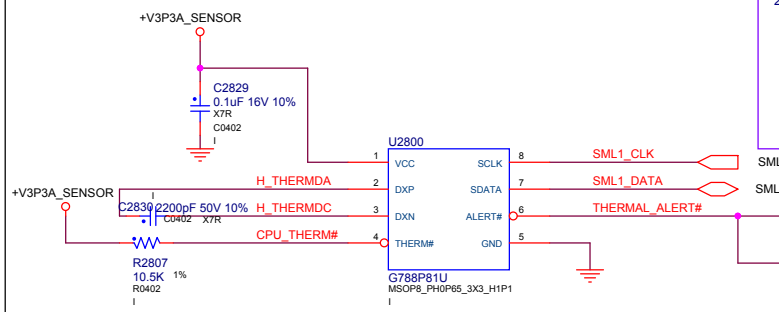
SENSORS

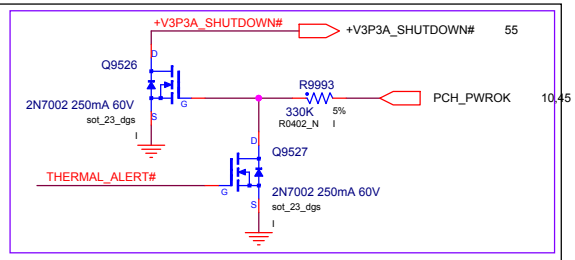




20170316 Added

CPU THERMAL SENSOR





20161220 :Added

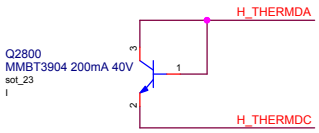
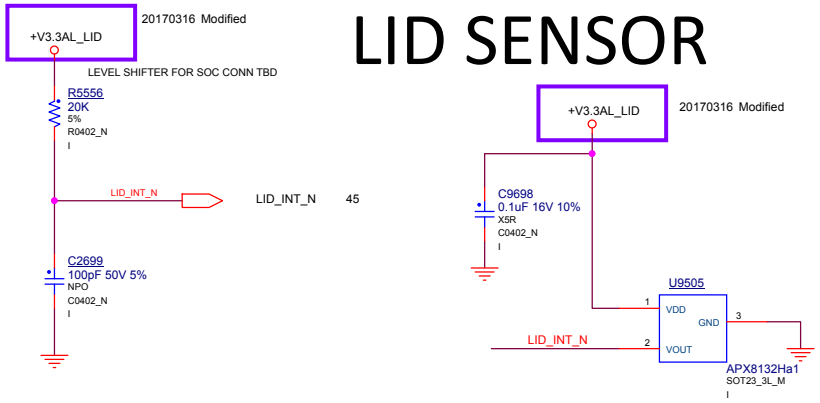


Table 10. Remote temperature $\overline{\text{THERM}}$ limit

The default value is trapping after power up 100ms by different pull-up resistors of $\overline{\text{THERM}}$ and $\overline{\text{ALERT}}$ pin:

TEMPERATURE (°C)		$\overline{\text{THERM}}$				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

LID SENSOR



INTERNAL ONLY

BPAGE DRAWING

apl_ff.GND
Fri May 27 06:47:20 2016

3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: <SENSORS>	Rev: V01
Date: Thursday, March 16, 2017	Sheet 26 of 63	

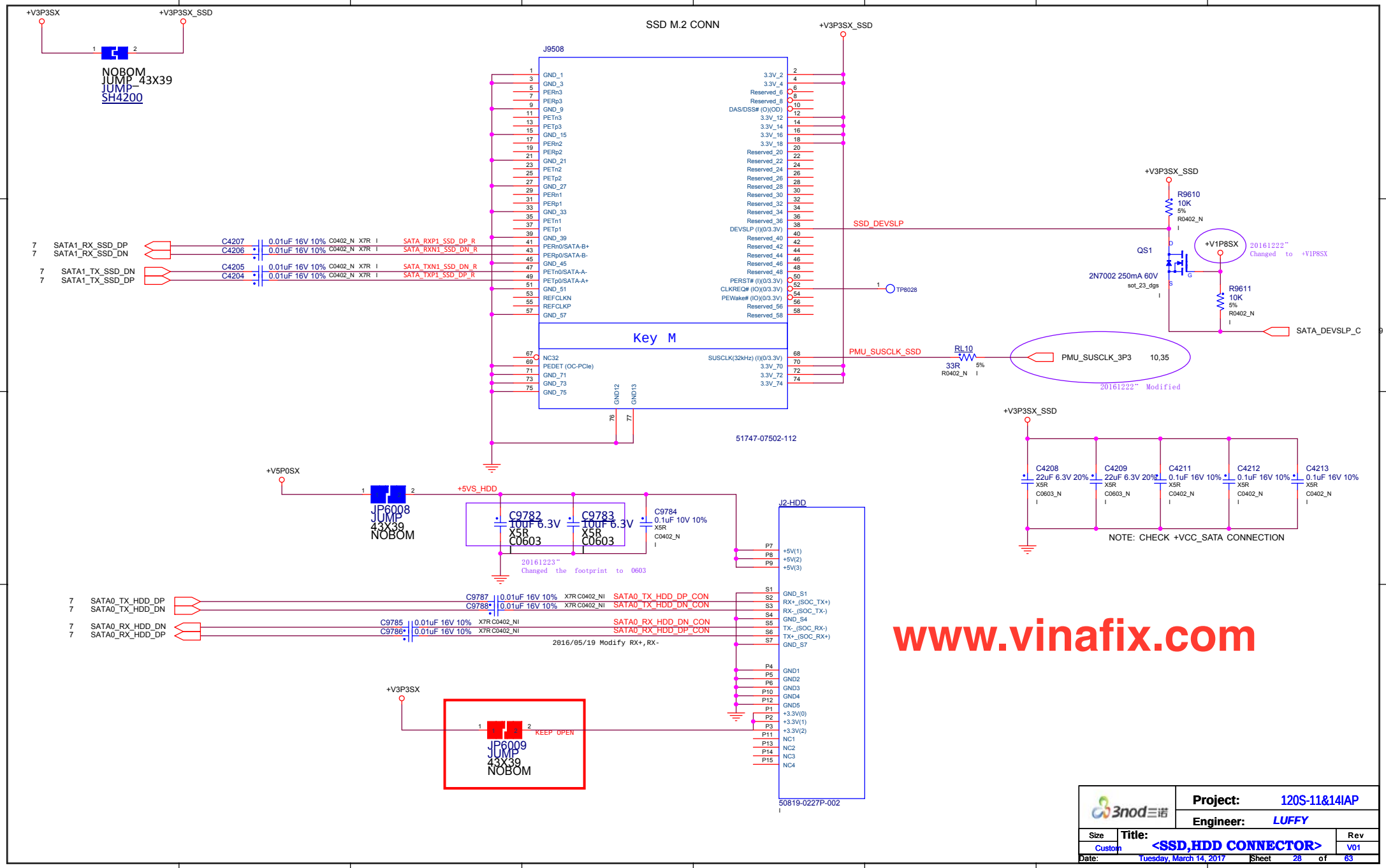
INTERNAL ONLY

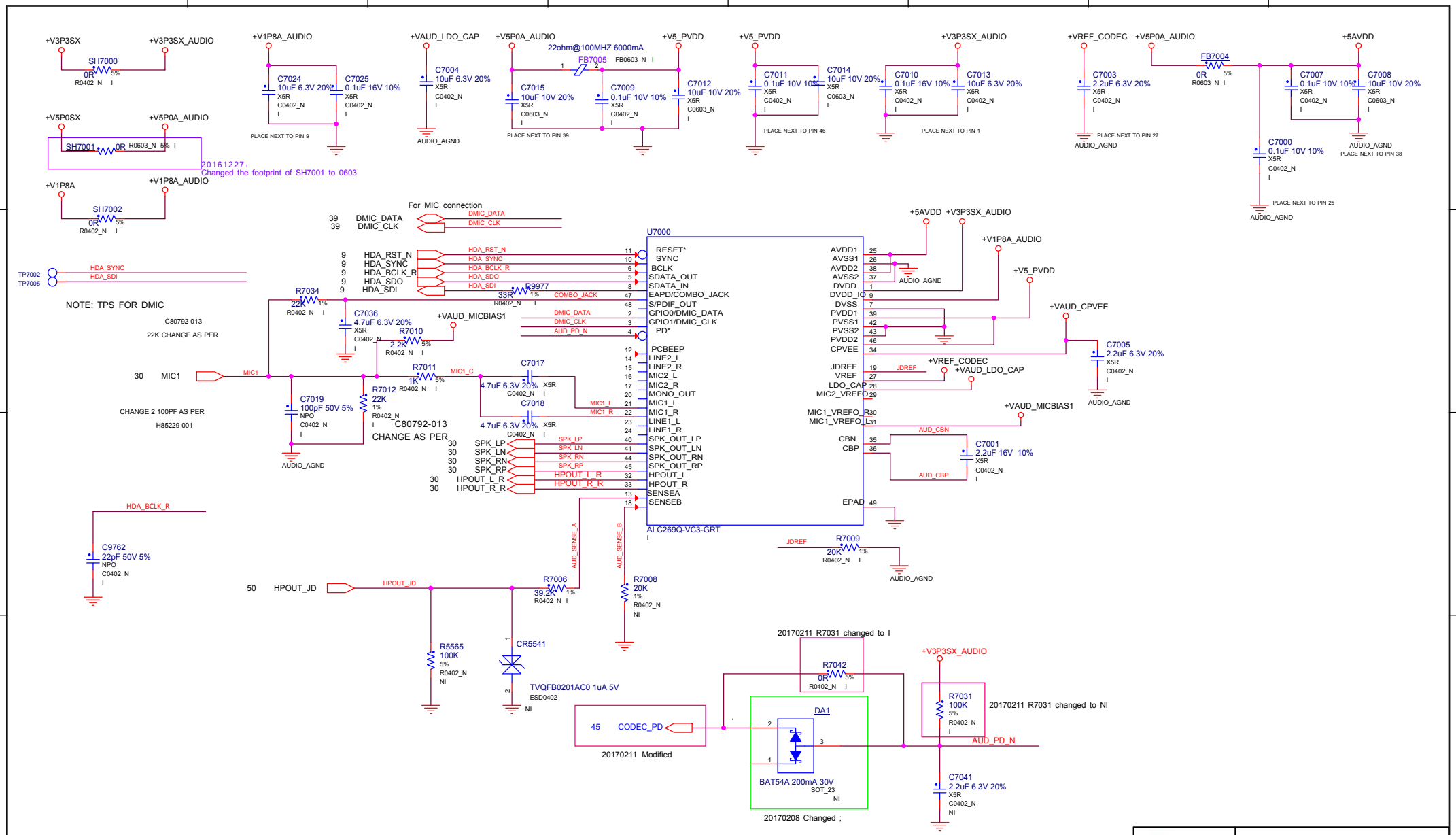
BPAGE DRAWING

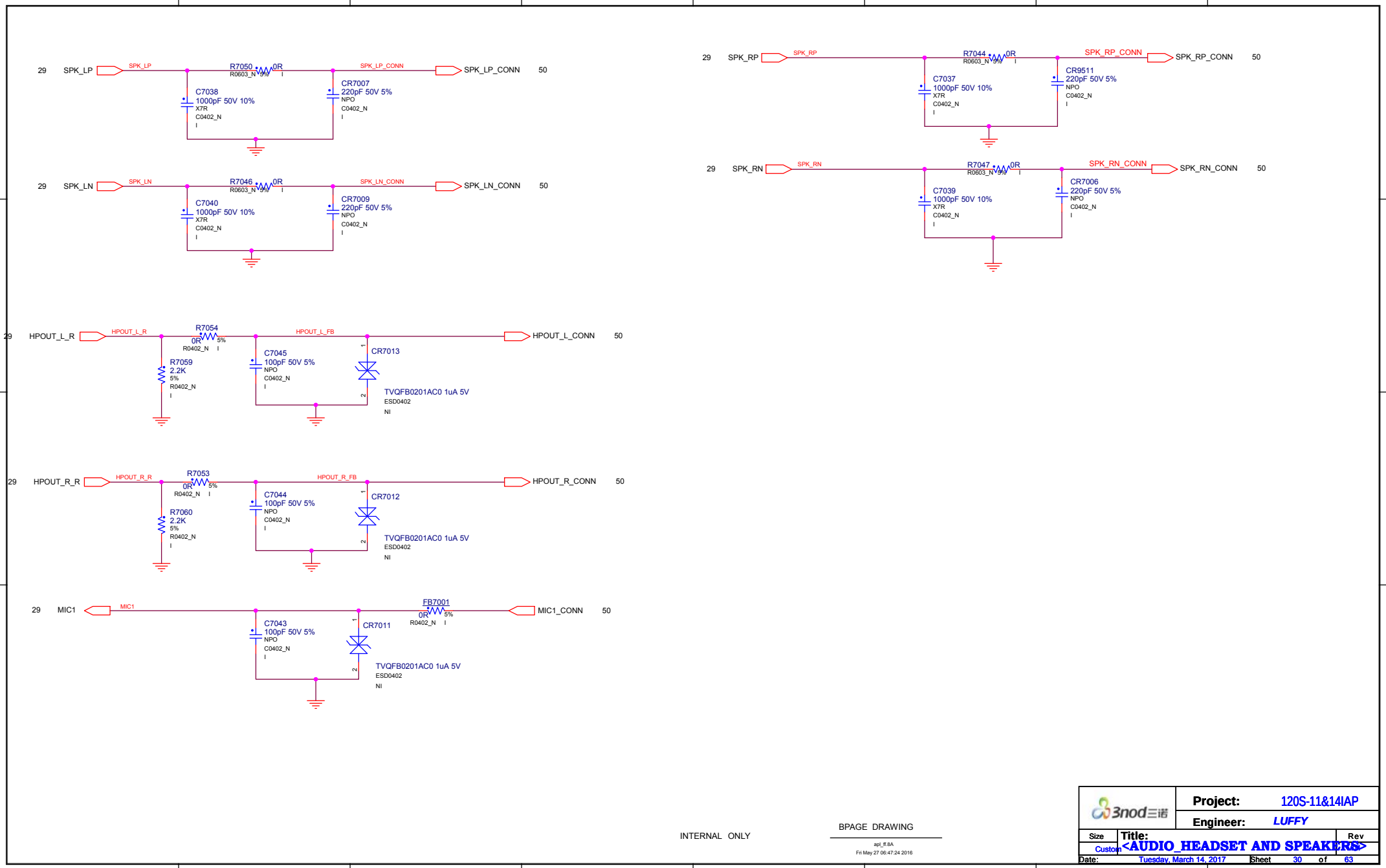
a p l _ f f.

Fri May 27 06:47:22 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title:	<NC>
		Rev: V01
Date:	Tuesday, March 14, 2017	Sheet 27 of 63


SSD M.2 CONN
J9508
Key M
51747-07502-112
+V3P3SX
+V3P3SX_SSD
NOBOM
JUMP_43X39
JUMP
SH4200
SATA1_RX_SSD_DP
SATA1_RX_SSD_DN
SATA1_TX_SSD_DN
SATA1_TX_SSD_DP
C4207 0.01uF 16V 10% C0402_N X7R
C4206 0.01uF 16V 10% C0402_N X7R
C4205 0.01uF 16V 10% C0402_N X7R
C4204 0.01uF 16V 10% C0402_N X7R
SATA_RXP1_SSD_DP_R
SATA_RXN1_SSD_DN_R
SATA_TXN1_SSD_DN_R
SATA_TXP1_SSD_DP_R
SSD_DEVSLP
TP8028
PMU_SUSCLK_SSD
RL10
33R
R0402_N
PMU_SUSCLK_3P3 10,35
20161222" Modified
R9610
10K
R0402_N
QS1
2N7002 250mA 60V
sot_23_dgs
+V1P8SX
20161222" Changed to +V1P8SX
R9611
10K
R0402_N
SATA_DEVSLP_C
+V5P0SX
JP6008
JUMP
43X39
NOBOM
+5VS_HDD
C9782 10uF 6.3V X5R C0603
C9783 10uF 6.3V X5R C0603
C9784 0.1uF 10V 10% X5R C0402_N
20161223" Changed the footprint to 0603
J2-HDD
50819-0227P-002
C4208 22uF 6.3V 20% X5R C0603_N
C4209 22uF 6.3V 20% X5R C0603_N
C4211 0.1uF 16V 10% X5R C0402_N
C4212 0.1uF 16V 10% X5R C0402_N
C4213 0.1uF 16V 10% X5R C0402_N
NOTE: CHECK +VCC_SATA CONNECTION
SATA0_TX_HDD_DP
SATA0_TX_HDD_DN
SATA0_RX_HDD_DN
SATA0_RX_HDD_DP
C9787 0.01uF 16V 10% X7R C0402_NI
C9788 0.01uF 16V 10% X7R C0402_NI
C9785 0.01uF 16V 10% X7R C0402_NI
C9786 0.01uF 16V 10% X7R C0402_NI
SATA0_TX_HDD_DP_CON
SATA0_TX_HDD_DN_CON
SATA0_RX_HDD_DN_CON
SATA0_RX_HDD_DP_CON
2016/05/19 Modify RX+,RX-
JP6009
JUMP
43X39
NOBOM
KEEP OPEN
www.vinafix.com
Project: 120S-11&14IAP
Engineer: LUFFY
Size: Custom
Title: <SSD,HDD CONNECTOR>
Rev: V01
Date: Tuesday, March 14, 2017
Sheet 28 of 63


+V3P3SX
+V3P3SX_AUDIO
SH7000
0R
R0402_N
+V5P0SX
+V5P0A_AUDIO
SH7001
0R R0603_N
20161227:
Changed the footprint of SH7001 to 0603
+V1P8A
+V1P8A_AUDIO
SH7002
0R
R0402_N
+V1P8A_AUDIO
C7024
10uF 6.3V 20%
C7025
0.1uF 16V 10%
PLACE NEXT TO PIN 9
+VAUD_LDO_CAP
C7004
10uF 6.3V 20%
AUDIO_AGND
+V5P0A_AUDIO
22ohm@100MHZ 6000mA
FB7005
FB0603_N
C7015
10uF 10V 20%
C7009
0.1uF 10V 10%
PLACE NEXT TO PIN 39
+V5_PVDD
C7012
10uF 10V 20%
+V5_PVDD
C7011
0.1uF 10V 10%
C7014
10uF 10V 20%
PLACE NEXT TO PIN 46
+V3P3SX_AUDIO
C7010
0.1uF 16V 10%
C7013
10uF 6.3V 20%
PLACE NEXT TO PIN 1
+VREF_CODEC
C7003
2.2uF 6.3V 20%
PLACE NEXT TO PIN 27
AUDIO_AGND
+V5P0A_AUDIO
FB7004
0R
R0603_N
C7000
0.1uF 10V 10%
PLACE NEXT TO PIN 25
+5AVDD
C7007
0.1uF 10V 10%
C7008
10uF 10V 20%
AUDIO_AGND
PLACE NEXT TO PIN 38
For MIC connection
39 DMIC_DATA
39 DMIC_CLK
DMIC_DATA
DMIC_CLK
TP7002
TP7005
HDA_SYNC
HDA_SDI
NOTE: TPS FOR DMIC
C80792-013
22K CHANGE AS PER
9 HDA_RST_N
9 HDA_SYNC
9 HDA_BCLK_R
9 HDA_SDO
9 HDA_SDI
R9977
33R
COMBO_JACK
R7034
22K
C7036
4.7uF 6.3V 20%
+VAUD_MICBIAS1
R7010
2.2K
30 MIC1
MIC1
R7011
1K
MIC1_C
C7017
4.7uF 6.3V 20%
C7018
4.7uF 6.3V 20%
C7019
100pF 50V 5%
R7012
22K
CHANGE 2 100PF AS PER
H85229-001
C80792-013
CHANGE AS PER
AUDIO_AGND
30 SPK_LP
30 SPK_LN
30 SPK_RN
30 SPK_RP
30 HPOUT_L_R
30 HPOUT_R_R
U7000
RESET*
SYNC
BCLK
SDATA_OUT
SDATA_IN
EAPD/COMBO_JACK
S/PDIF_OUT
GPIO0/DMIC_DATA
GPIO1/DMIC_CLK
PD*
PCBEEP
LINE2_L
LINE2_R
MIC2_L
MIC2_R
MONO_OUT
MIC1_L
MIC1_R
LINE1_L
LINE1_R
SPK_OUT_LP
SPK_OUT_LN
SPK_OUT_RN
SPK_OUT_RP
HPOUT_L
HPOUT_R
SENSEA
SENSEB
ALC269Q-VC3-GRT
AVDD1
AVSS1
AVDD2
AVSS2
DVDD
DVDD_IO
DVSS
PVDD1
PVSS1
PVSS2
PVDD2
CPVEE
JDREF
VREF
LDO_CAP
MIC2_VREFO
MIC1_VREFO_R
MIC1_VREFO_L
CBN
CBP
EPAD
+5AVDD
+V3P3SX_AUDIO
+V1P8A_AUDIO
+V5_PVDD
+VAUD_CPVEE
C7005
2.2uF 6.3V 20%
+VREF_CODEC
+VAUD_LDO_CAP
+VAUD_MICBIAS1
C7001
2.2uF 16V 10%
AUD_CBN
AUD_CBP
R7009
20K
HDA_BCLK_R
C9762
22pF 50V 5%
50 HPOUT_JD
HPOUT_JD
R7006
39.2K
AUD_SENSE_A
AUD_SENSE_B
R7008
20K
R5565
100K
CR5541
TVQFB0201AC0 1uA 5V
ESD0402
20170211 R7031 changed to I
R7042
0R
+V3P3SX_AUDIO
R7031
100K
20170211 R7031 changed to NI
45 CODEC_PD
20170211 Modified
DA1
BAT54A 200mA 30V
SOT_23
20170208 Changed ;
AUD_PD_N
C7041
2.2uF 6.3V 20%
INTERNAL ONLY
BPAGE DRAWING
Project: 120S-11&14IAP
Engineer: LUFFY
Size Custom
Title: <AUDIO CODEC>
Rev V01
Date: Tuesday, March 14, 2017
Sheet 29 of 63

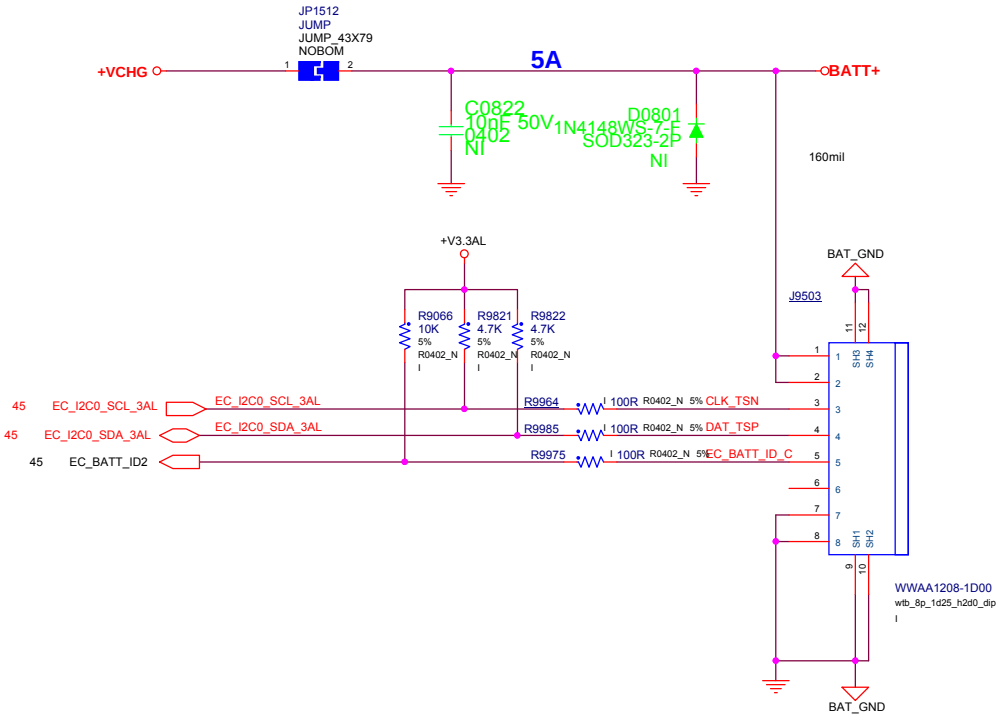


INTERNAL ONLY

BPAGE DRAWING

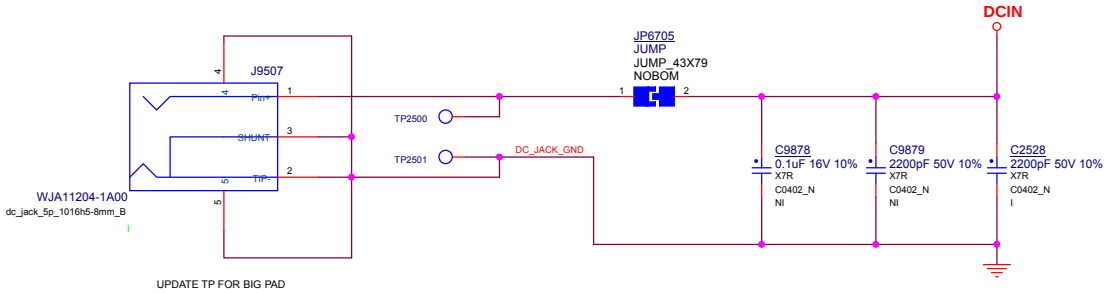
apl_IE.8A
Fri May 27 06:47:24 2016

3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: <AUDIO_HEADSET AND SPEAKERS>	Rev
Date: Tuesday, March 14, 2017	Sheet 30 of 63	



20170205 Deleted reserved design for dummy battery

3nod三诺	Project: 120S-11&14IAP	
	Engineer: GGS	
Size: Custom	Title: <GAUGE&BATTERY CONN>	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 31 of 63	



UPDATE TP FOR BIG PAD

INTERNAL ONLY

BPAGE DRAWING

apl_ff.ADP_P.48
Fri May 27 06:47:24 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	GGS
Size: Custom	Title: <DC JACK>	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 32 of 63	

INTERNAL ONLY

BPAGE DRAWING

apl_ff.8A
Fri May 27 06:47:24 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: <NC>	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 33 of 63	

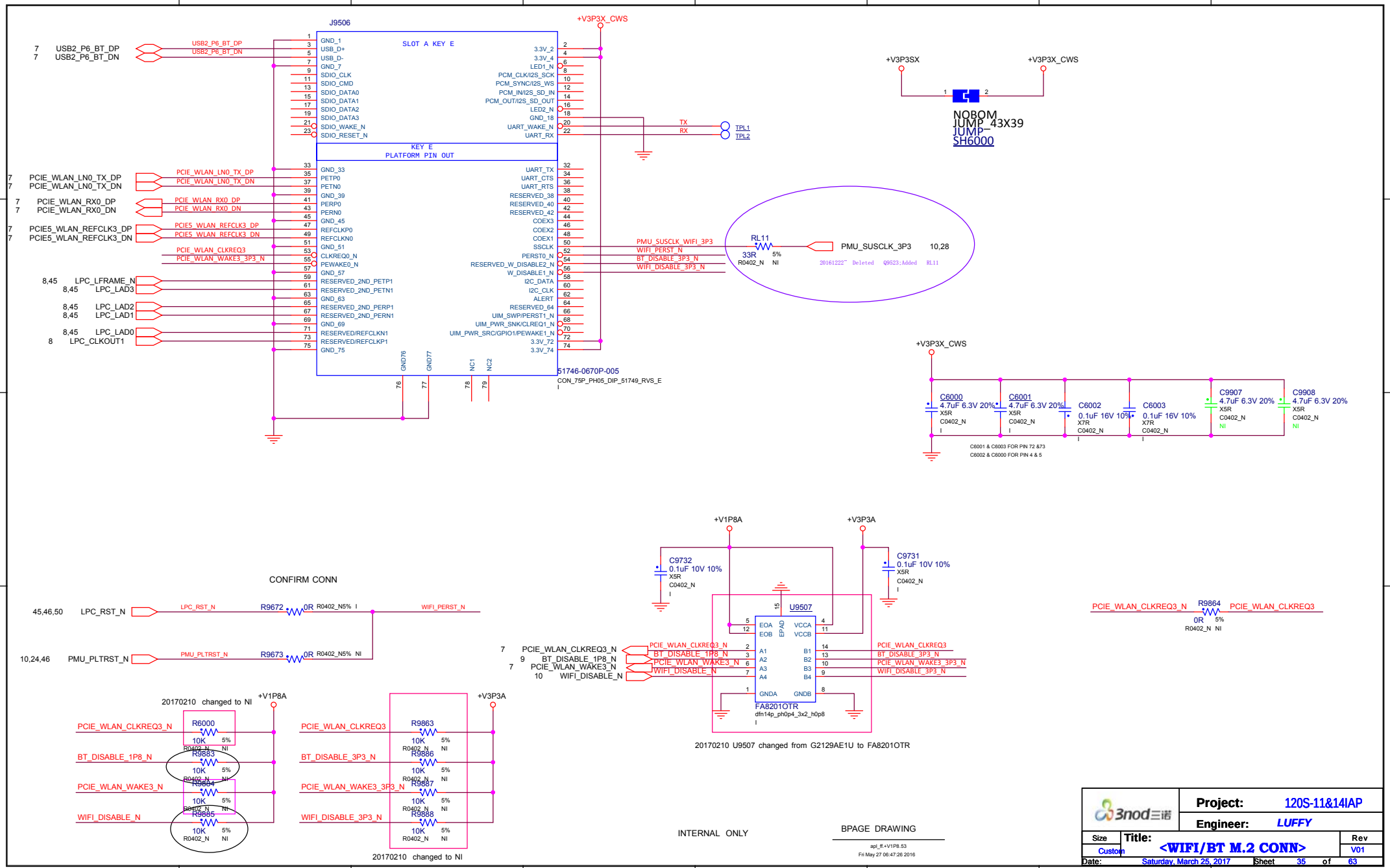
INTERNAL ONLY

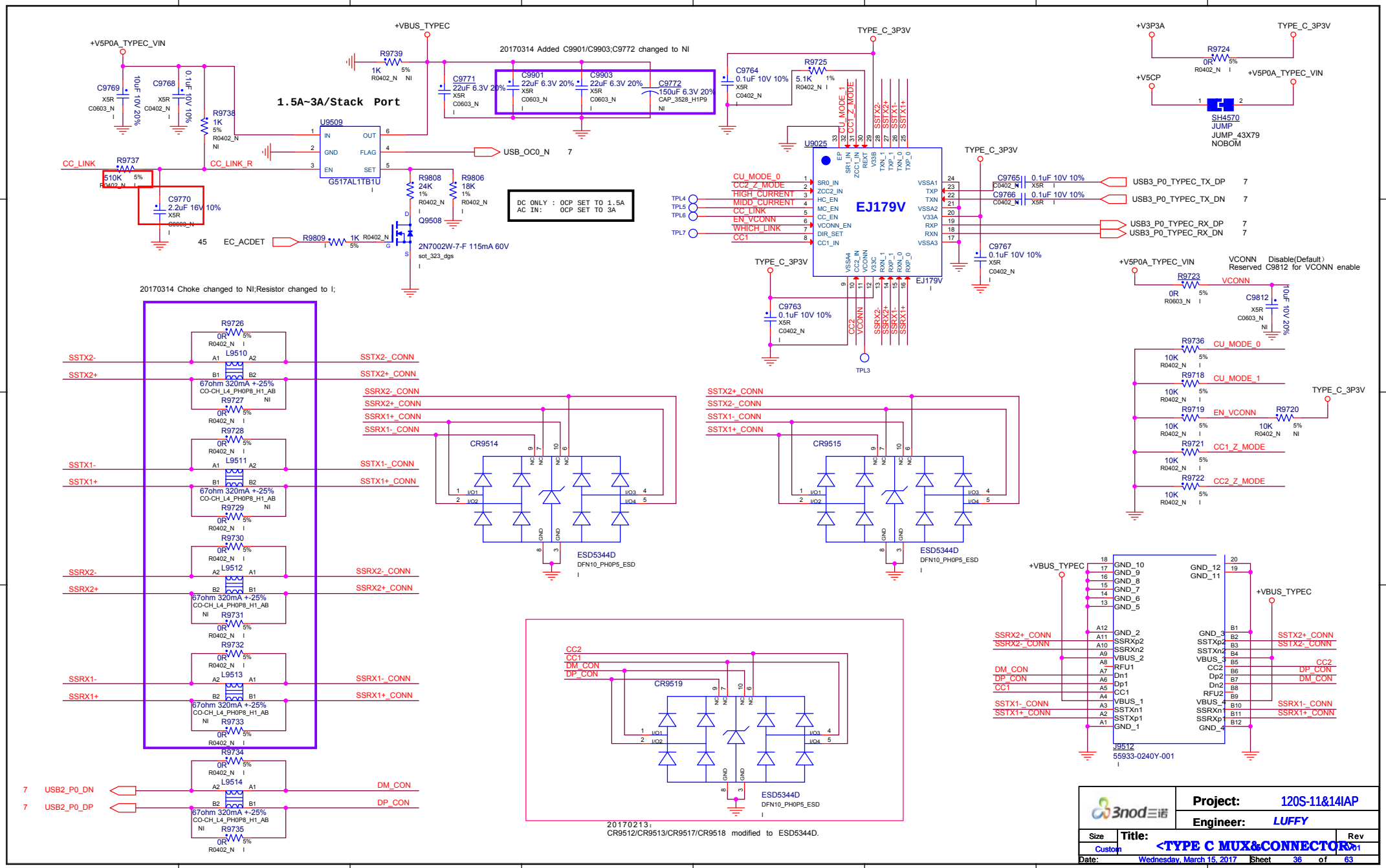
BPAGE DRAWING

apl_ff.
Fri May 27 06:47:24 2016

TYPE-C PD CONTROLLER

3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: <NC>	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 34 of 63	


J9506
SLOT A KEY E
KEY E
PLATFORM PIN OUT
+V3P3X_CWS
7 USB2_P6_BT_DP
7 USB2_P6_BT_DN
USB2_P6_BT_DP
USB2_P6_BT_DN
7 PCIE_WLAN_LN0_TX_DP
7 PCIE_WLAN_LN0_TX_DN
PCIE_WLAN_LN0_TX_DP
PCIE_WLAN_LN0_TX_DN
7 PCIE_WLAN_RX0_DP
7 PCIE_WLAN_RX0_DN
PCIE_WLAN_RX0_DP
PCIE_WLAN_RX0_DN
7 PCIE5_WLAN_REFCLK3_DP
7 PCIE5_WLAN_REFCLK3_DN
PCIE5_WLAN_REFCLK3_DP
PCIE5_WLAN_REFCLK3_DN
PCIE_WLAN_CLKREQ3
PCIE_WLAN_WAKE3_3P3_N
8,45 LPC_LFRAME_N
8,45 LPC_LAD3
8,45 LPC_LAD2
8,45 LPC_LAD1
8,45 LPC_LAD0
8 LPC_CLKOUT1
TX
RX
TPL1
TPL2
PMU_SUSCLK_WIFI_3P3
WIFI_PERST_N
BT_DISABLE_3P3_N
WIFI_DISABLE_3P3_N
RL11
33R 5%
R0402_N NI
PMU_SUSCLK_3P3 10,28
20161222 Deleted Q9523;Added RL11
51746-0670P-005
CON_75P_PH05_DIP_51749_RVS_E
+V3P3SX
+V3P3X_CWS
NOBOM
JUMP_43X39
JUMP
SH6000
C6000 4.7uF 6.3V 20% X5R C0402_N
C6001 4.7uF 6.3V 20% X5R C0402_N
C6002 0.1uF 16V 10% X7R C0402_N
C6003 0.1uF 16V 10% X7R C0402_N
C9907 4.7uF 6.3V 20% X5R C0402_N NI
C9908 4.7uF 6.3V 20% X5R C0402_N NI
C6001 & C6003 FOR PIN 72 &73
C6002 & C6000 FOR PIN 4 & 5
CONFIRM CONN
45,46,50 LPC_RST_N
LPC_RST_N
R9672 0R R0402_N5% I
WIFI_PERST_N
10,24,46 PMU_PLTRST_N
PMU_PLTRST_N
R9673 0R R0402_N5% NI
+V1P8A
+V3P3A
C9732 0.1uF 10V 10% X5R C0402_N
C9731 0.1uF 10V 10% X5R C0402_N
U9507
FA8201OTR
7 PCIE_WLAN_CLKREQ3_N
9 BT_DISABLE_1P8_N
7 PCIE_WLAN_WAKE3_N
10 WIFI_DISABLE_N
PCIE_WLAN_CLKREQ3
BT_DISABLE_3P3_N
PCIE_WLAN_WAKE3_3P3_N
WIFI_DISABLE_3P3_N
PCIE_WLAN_CLKREQ3_N
R9864 0R 5% R0402_N NI
PCIE_WLAN_CLKREQ3
20170210 changed to NI
R6000 10K 5% R0402_N NI
R9883 10K 5% R0402_N NI
R9884 10K 5% R0402_N NI
R9885 10K 5% R0402_N NI
R9863 10K 5% R0402_N NI
R9886 10K 5% R0402_N NI
R9887 10K 5% R0402_N NI
R9888 10K 5% R0402_N NI
20170210 changed to NI
20170210 U9507 changed from G2129AE1U to FA8201OTR
INTERNAL ONLY
BPAGE DRAWING
Project: 120S-11&14IAP
Engineer: LUFFY
Size Custom
Title: <WIFI/BT M.2 CONN>
Rev V01
Date: Saturday, March 25, 2017
Sheet 35 of 63


+V5P0A_TYPEC_VIN
C9769 10uF 10V 20% X5R C0603_N
C9768 0.1uF 10V 10% X5R C0402_N
R9738 1K 5% R0402_N NI
1.5A~3A/Stack Port
U9509
IN OUT GND FLAG EN SET
G517AL1TB1U
+VBUS_TYPEC
R9739 1K 5% R0402_N NI
C9771 22uF 6.3V 20% X5R C0603_N
C9901 22uF 6.3V 20% X5R C0603_N
C9903 22uF 6.3V 20% X5R C0603_N
C9772 150uF 6.3V 20% CAP_3528_H1P9 NI
20170314 Added C9901/C9903;C9772 changed to NI
USB_OC0_N 7
CC_LINK
R9737 510K 5% R0402_N
CC_LINK_R
C9770 2.2uF 16V 10% X5R C0603_N
R9808 24K 1% R0402_N
R9806 18K 1% R0402_N
Q9508
2N7002W-7-F 115mA 60V
sot_323_dgs
45 EC_ACDET
R9809 1K 5% R0402_N
DC ONLY : OCP SET TO 1.5A
AC IN: OCP SET TO 3A
TYPE_C_3P3V
C9764 0.1uF 10V 10% X5R C0402_N
R9725 5.1K 1% R0402_N
U9025
EJ179V
CU_MODE_0
CC2_Z_MODE
HIGH_CURRENT
MIDD_CURRENT
CC_LINK
EN_VCONN
WHICH_LINK
CC1
TPL4
TPL5
TPL6
TPL7
C9765 0.1uF 10V 10% X5R C0402_N
C9766 0.1uF 10V 10% X5R C0402_N
USB3_P0_TYPEC_TX_DP 7
USB3_P0_TYPEC_TX_DN 7
USB3_P0_TYPEC_RX_DP 7
USB3_P0_TYPEC_RX_DN 7
C9767 0.1uF 10V 10% X5R C0402_N
C9763 0.1uF 10V 10% X5R C0402_N
TPL3
+V3P3A
R9724 0R 5% R0402_N
+V5CP
SH4570
JUMP
JUMP_43X79
NOBOM
+V5P0A_TYPEC_VIN
R9723 0R 5% R0603_N
VCONN
C9812 10uF 10V 20% X5R C0603_N NI
VCONN Disable(Default)
Reserved C9812 for VCONN enable
R9736 10K 5% R0402_N CU_MODE_0
R9718 10K 5% R0402_N CU_MODE_1
R9719 10K 5% R0402_N EN_VCONN
R9720 10K 5% R0402_N NI
R9721 10K 5% R0402_N CC1_Z_MODE
R9722 10K 5% R0402_N CC2_Z_MODE
20170314 Choke changed to NI;Resistor changed to I;
R9726 0R 5% R0402_N
L9510
SSTX2- SSTX2+
SSTX2-_CONN SSTX2+_CONN
67ohm 320mA +-25% CO-CH_L4_PH0P8_H1_AB
R9727 0R 5% R0402_N
R9728 0R 5% R0402_N
L9511
SSTX1- SSTX1+
SSTX1-_CONN SSTX1+_CONN
R9729 0R 5% R0402_N
R9730 0R 5% R0402_N
L9512
SSRX2- SSRX2+
SSRX2-_CONN SSRX2+_CONN
R9731 0R 5% R0402_N
R9732 0R 5% R0402_N
L9513
SSRX1- SSRX1+
SSRX1-_CONN SSRX1+_CONN
R9733 0R 5% R0402_N
R9734 0R 5% R0402_N
L9514
7 USB2_P0_DN
7 USB2_P0_DP
DM_CON DP_CON
R9735 0R 5% R0402_N
CR9514
CR9515
ESD5344D DFN10_PH0P5_ESD
CR9519
CC2 CC1 DM_CON DP_CON
20170213:
CR9512/CR9513/CR9517/CR9518 modified to ESD5344D.
J9512
55933-0240Y-001
GND_10 GND_9 GND_8 GND_7 GND_6 GND_5 GND_2 SSRXp2 SSRXn2 VBUS_2 RFU1 Dn1 Dp1 CC1 VBUS_1 SSTXn1 SSTXp1 GND_1
GND_12 GND_11 GND_3 SSTXp2 SSTXn2 VBUS_3 CC2 Dp2 Dn2 RFU2 VBUS_4 SSRXn1 SSRXp1 GND_4
Project: 120S-11&14IAP
Engineer: LUFFY
Size Custom
Title: <TYPE C MUX&CONNECTOR>
Rev 0.01
Date: Wednesday, March 15, 2017
Sheet 36 of 63

HDMI LEVEL SHIFTER

+V1P8A — NOBOM (JUMP_43X39, SH9500, JUMP) — +V1P8A_HDMI

6 DDI0_TX0_DP — DDI0_TX0_DP — C9580 0.1uF 10V 10% C0402_N X5R — HDMI_TX2_CMC_DP
6 DDI0_TX0_DN — DDI0_TX0_DN — C9581 0.1uF 10V 10% C0402_N X5R — HDMI_TX2_CMC_DN
6 DDI0_TX1_DP — DDI0_TX1_DP — C9582 0.1uF 10V 10% C0402_N X5R — HDMI_TX1_CMC_DP
6 DDI0_TX1_DN — DDI0_TX1_DN — C9583 0.1uF 10V 10% C0402_N X5R — HDMI_TX1_CMC_DN
6 DDI0_TX2_DP — DDI0_TX2_DP — C9584 0.1uF 10V 10% C0402_N X5R — HDMI_TX0_CMC_DP
6 DDI0_TX2_DN — DDI0_TX2_DN — C9585 0.1uF 10V 10% C0402_N X5R — HDMI_TX0_CMC_DN
6 DDI0_TX3_DP — DDI0_TX3_DP — C9586 0.1uF 10V 10% C0402_N X5R — HDMI_CLK_CMC_DP
6 DDI0_TX3_DN — DDI0_TX3_DN — C9587 0.1uF 10V 10% C0402_N X5R — HDMI_CLK_CMC_DN

R9528 0R 5% R0402_N NI — HDMI_TX2_CMC_DP / HDMI_TX2_CMC_DN — L4S12X20U 90ohm 100mA +-20% L9508 — HDMI_TX2_CONN_DP / HDMI_TX2_CONN_DN — HDMI_TX2_CONN_DP 38, HDMI_TX2_CONN_DN 38
R9529 0R 5% R0402_N

R9530 0R 5% R0402_N NI — HDMI_TX1_CMC_DP / HDMI_TX1_CMC_DN — L4S12X20U 90ohm 100mA +-20% L9509 — HDMI_TX1_CONN_DP / HDMI_TX1_CONN_DN — HDMI_TX1_CONN_DP 38, HDMI_TX1_CONN_DN 38
R9531 0R 5% R0402_N

R9532 0R 5% R0402_N NI — HDMI_TX0_CMC_DP / HDMI_TX0_CMC_DN — L4S12X20U 90ohm 100mA +-20% L9506 — HDMI_TX0_CONN_DP / HDMI_TX0_CONN_DN — HDMI_TX0_CONN_DP 38, HDMI_TX0_CONN_DN 38
R9533 0R 5% R0402_N

R9534 0R 5% R0402_N NI — HDMI_CLK_CMC_DP / HDMI_CLK_CMC_DN — L4S12X20U 90ohm 100mA +-20% L9507 — HDMI_CLK_CONN_DP / HDMI_CLK_CONN_DN — HDMI_CLK_CONN_DP 38, HDMI_CLK_CONN_DN 38
R9535 0R 5% R0402_N

+V5P0SX_HDMI — CR9500 BAT54A 200mA 30V SOT_23 — VHDMI_SCL, VHDMI_SDA
R9577 2.2K 5% R0402_N — R9580 2.2K 5% R0402_N
38 HDMI_DDC_SCL — HDMI_DDC_SDA 38

+V1P8A_HDMI — Q9501 BSS138 300mA 50V sot23_gsd — Q9503 BSS138 300mA 50V sot23_gsd
R9579 2.2K 5% R0402_N — R9581 2.2K 5% R0402_N
6 DDI0_DDC_SCL — DDI0_DDC_SCL
6 DDI0_DDC_SDA — DDI0_DDC_SDA

HDMI_PLS_FET — Q9504 2N7002W-7-F 115mA 60V sot_323_dgs
40,45 EC_SLP_SX — R9682 100K 5% R0402_N

+V1P8A_HDMI — R9578 10K 5% R0402_N — DDI0_HPD_N — DDI0_HPD_N 6
Q9502 2N7002W-7-F 115mA 60V sot_323_dgs — HDMI_HPD — HDMI_HPD 38
R9576 100K 5% R0402_N

FET HAS BEEN CHANGED PLEASE REVIEW

HDMI_TX2_CMC_DP / HDMI_TX2_CMC_DN
HDMI_TX1_CMC_DP / HDMI_TX1_CMC_DN
HDMI_TX0_CMC_DP / HDMI_TX0_CMC_DN
HDMI_CLK_CMC_DP / HDMI_CLK_CMC_DN

20161228:
Changed from 680R to 470R

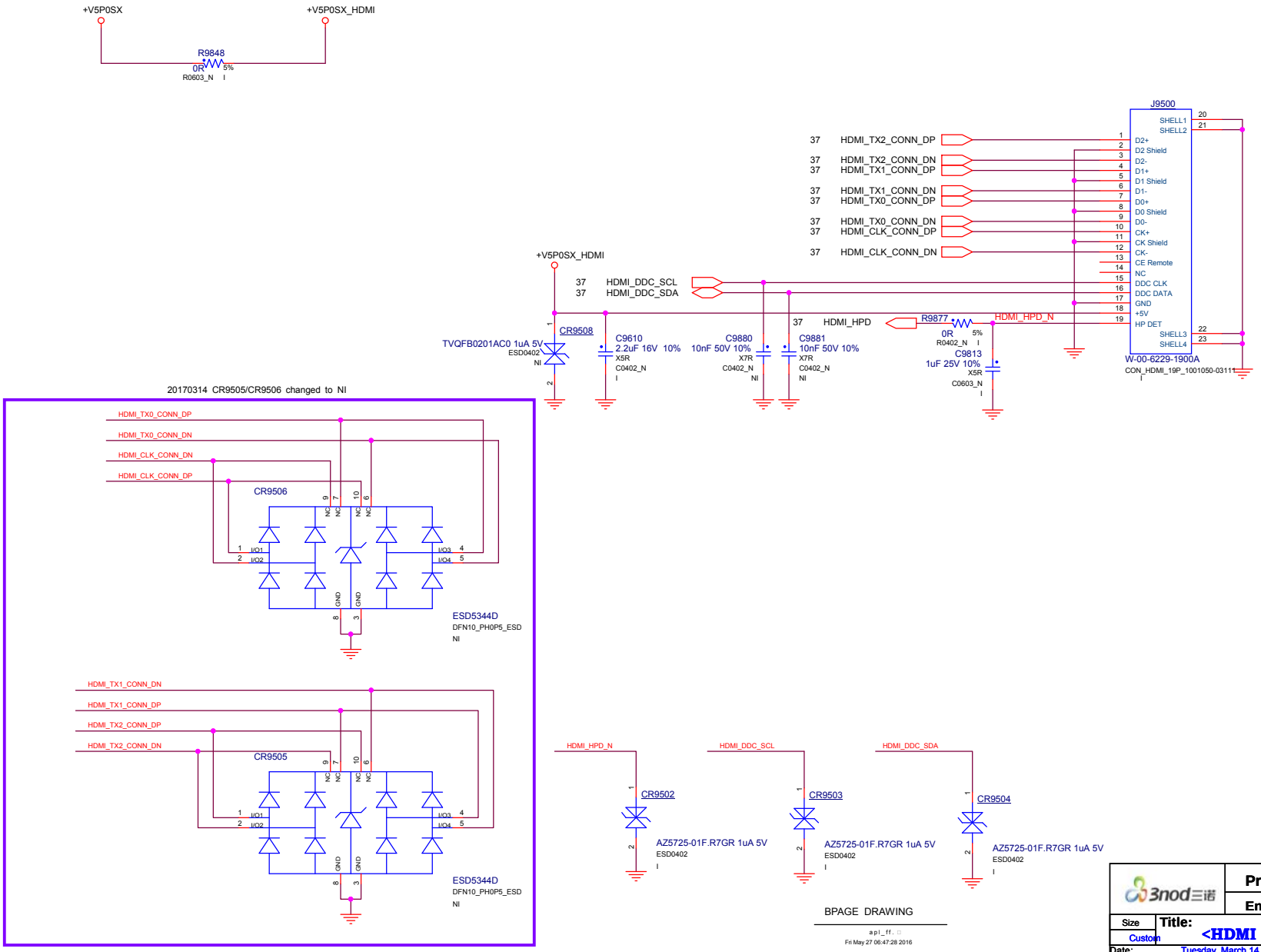
R9520 470R 1% R0402_N — R9521 470R 1% R0402_N — R9522 470R 1% R0402_N — R9523 470R 1% R0402_N — R9524 470R 1% R0402_N — R9525 470R 1% R0402_N — R9526 470R 1% R0402_N — R9527 470R 1% R0402_N

HDMI_PLS_FET

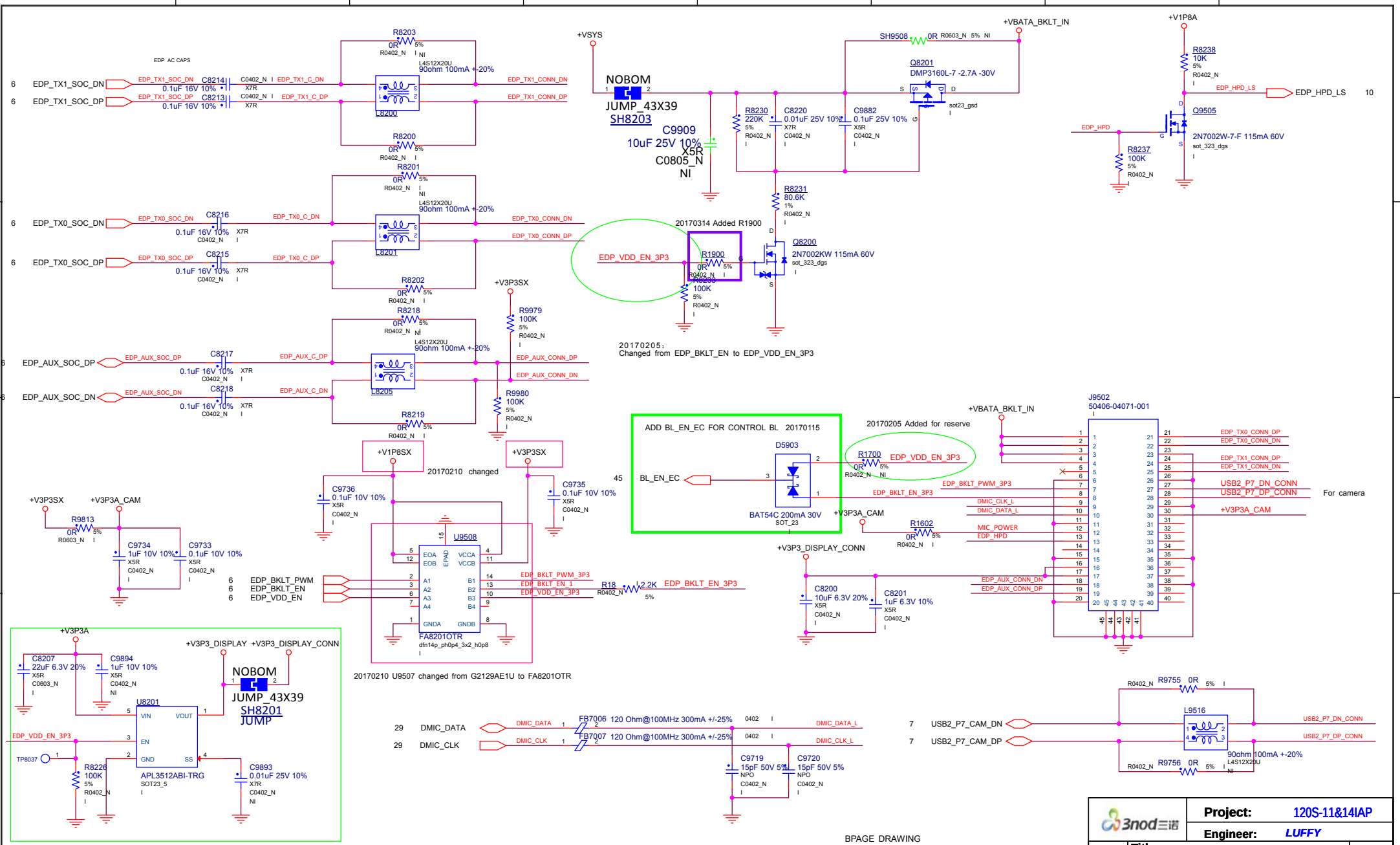
BPAGE DRAWING
apl_IE.8A
Fri May 27 06:47:26 2016

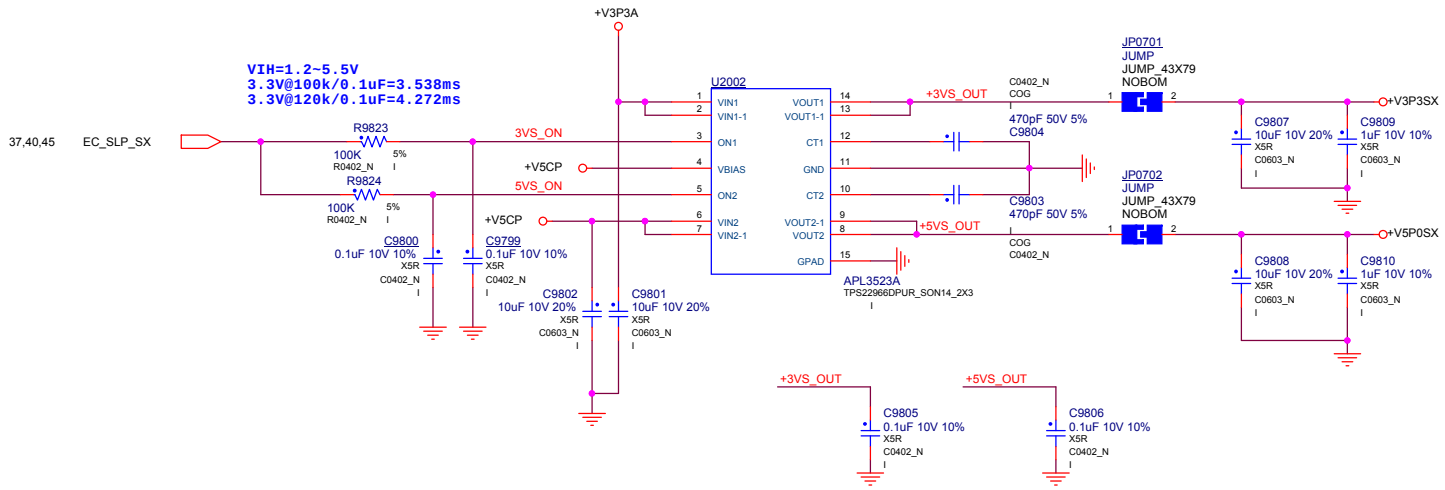
3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: <HDMI LEVEL SHIFTER>	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 37 of 63	

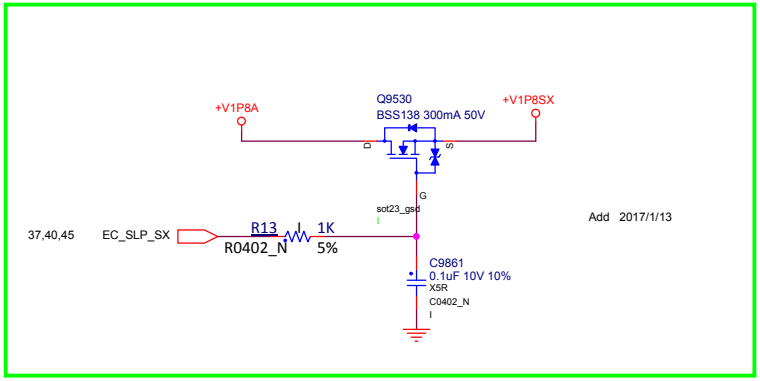
HDMI CONNECTOR



3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: <HDMI CONN>	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 38 of 63	


EDP AC CAPS
EDP_TX1_SOC_DN
EDP_TX1_SOC_DP
C8214 0.1uF 16V 10% X7R C0402_N
C8213 0.1uF 16V 10% X7R C0402_N
EDP_TX1_C_DN
EDP_TX1_C_DP
R8203 0R R0402_N 5% NI
R8200 0R R0402_N 5% I
L4S12X20U 90ohm 100mA +-20%
L8200
EDP_TX1_CONN_DN
EDP_TX1_CONN_DP
EDP_TX0_SOC_DN
EDP_TX0_SOC_DP
C8216 0.1uF 16V 10% X7R C0402_N
C8215 0.1uF 16V 10% X7R C0402_N
EDP_TX0_C_DN
EDP_TX0_C_DP
R8201 0R R0402_N 5% I NI
R8202 0R R0402_N 5% I
L8201
EDP_TX0_CONN_DN
EDP_TX0_CONN_DP
EDP_AUX_SOC_DP
EDP_AUX_SOC_DN
C8217 0.1uF 16V 10% X7R C0402_N
C8218 0.1uF 16V 10% X7R C0402_N
EDP_AUX_C_DP
EDP_AUX_C_DN
R8218 0R R0402_N 5% NI
R8219 0R R0402_N 5% I
L8205
EDP_AUX_CONN_DP
EDP_AUX_CONN_DN
+V3P3SX
R9979 100K 5% R0402_N
R9980 100K 5% R0402_N
+VSYS
NOBOM
JUMP_43X39
SH8203
C9909 10uF 25V 10% X5R C0805_N NI
R8230 220K 5% R0402_N
C8220 0.01uF 25V 10% X7R C0402_N
C9882 0.1uF 25V 10% X5R C0402_N
SH9508 0R R0603_N 5% NI
+VBATA_BKLT_IN
Q8201 DMP3160L-7 -2.7A -30V sot23_gsd
R8231 80.6K 1% R0402_N
20170314 Added R1900
EDP_VDD_EN_3P3
R1900 0R R0402_N 5%
R8233 100K 5% R0402_N
Q8200 2N7002KW 115mA 60V sot_323_dgs
20170205:
Changed from EDP_BKLT_EN to EDP_VDD_EN_3P3
+V1P8A
R8238 10K 5% R0402_N
EDP_HPD_LS
EDP_HPD_LS 10
Q9505 2N7002W-7-F 115mA 60V sot_323_dgs
EDP_HPD
R8237 100K 5% R0402_N
ADD BL_EN_EC FOR CONTROL BL 20170115
D5903 BAT54C 200mA 30V SOT_23
BL_EN_EC
R1700 0R R0402_N 5% NI
20170205 Added for reserve
+V1P8SX
+V3P3SX
20170210 changed
C9736 0.1uF 10V 10% X5R C0402_N
C9735 0.1uF 10V 10% X5R C0402_N
+V3P3SX
+V3P3A_CAM
R9813 0R R0603_N 5%
C9734 1uF 10V 10% X5R C0402_N
C9733 0.1uF 10V 10% X5R C0402_N
U9508
EOA EOB A1 A2 A3 A4 GNDA VCCA VCCB B1 B2 B3 B4 GNDB EPAD
FA8201OTR dfn14p_ph0p4_3x2_h0p8
EDP_BKLT_PWM
EDP_BKLT_EN
EDP_VDD_EN
EDP_BKLT_PWM_3P3
EDP_BKLT_EN_1
EDP_VDD_EN_3P3
R18 2.2K 5% R0402_N
EDP_BKLT_EN_3P3
20170210 U9507 changed from G2129AE1U to FA8201OTR
J9502 50406-04071-001
+VBATA_BKLT_IN
EDP_TX0_CONN_DP
EDP_TX0_CONN_DN
EDP_TX1_CONN_DP
EDP_TX1_CONN_DN
EDP_BKLT_PWM_3P3
EDP_BKLT_EN_3P3
DMIC_CLK_L
DMIC_DATA_L
MIC_POWER
EDP_HPD
USB2_P7_DN_CONN
USB2_P7_DP_CONN
+V3P3A_CAM
For camera
R1602 0R R0402_N 5%
+V3P3_DISPLAY_CONN
C8200 10uF 6.3V 20% X5R C0402_N
C8201 1uF 6.3V 10% X5R C0402_N
EDP_AUX_CONN_DN
EDP_AUX_CONN_DP
+V3P3A
C8207 22uF 6.3V 20% X5R C0603_N
C9894 1uF 10V 10% X5R C0402_N NI
+V3P3_DISPLAY
+V3P3_DISPLAY_CONN
NOBOM
JUMP_43X39
SH8201
JUMP
U8201
VIN VOUT EN GND SS
APL3512ABI-TRG SOT23_5
EDP_VDD_EN_3P3
TP8037
R8226 100K 5% R0402_N
C9893 0.01uF 25V 10% X7R C0402_N NI
20170207 U8201 changed from WS4601E-5/TR to APL3512ABI-TRG
DMIC_DATA
DMIC_CLK
FB7006 120 Ohm@100MHz 300mA +/-25% 0402
FB7007 120 Ohm@100MHz 300mA +/-25% 0402
DMIC_DATA_L
DMIC_CLK_L
C9719 15pF 50V 5% NPO C0402_N
C9720 15pF 50V 5% NPO C0402_N
USB2_P7_CAM_DN
USB2_P7_CAM_DP
R9755 0R R0402_N 5%
R9756 0R R0402_N 5%
L9516 90ohm 100mA +-20% L4S12X20U NI
USB2_P7_DN_CONN
USB2_P7_DP_CONN
INTERNAL ONLY
BPAGE DRAWING
Project: 120S-11&14IAP
Engineer: LUFFY
Size Custom
Title: <DISPLAY>
Rev V01
Date: Tuesday, March 28, 2017
Sheet 39 of 63





INTERNAL ONLY

BPAGE DRAWING

apl_lf.8A
Fri May 27 06:47:28 2016

3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: +V5P0A ,+V3P3SX,+V5P0SX	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 40 of 63	

[PAGE_TITLE= TI PMIC 1 OF 4]

BPAGE DRAWING

apl_ff.GND
Fri May 27 06:47:28 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: <NC>	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 41 of 63	

BPAGE DRAWING

apl_ff UNS13.137
Fri May 27 06:47:30 2016

3nod三诺	Project: 120S-11&14IAP	
	Engineer: *LUFFY*	
Size: Custom	Title: <NC>	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 42 of 63	

BPAGE DRAWING

apl_ff.8A
Fri May 27 06:47:30 2016

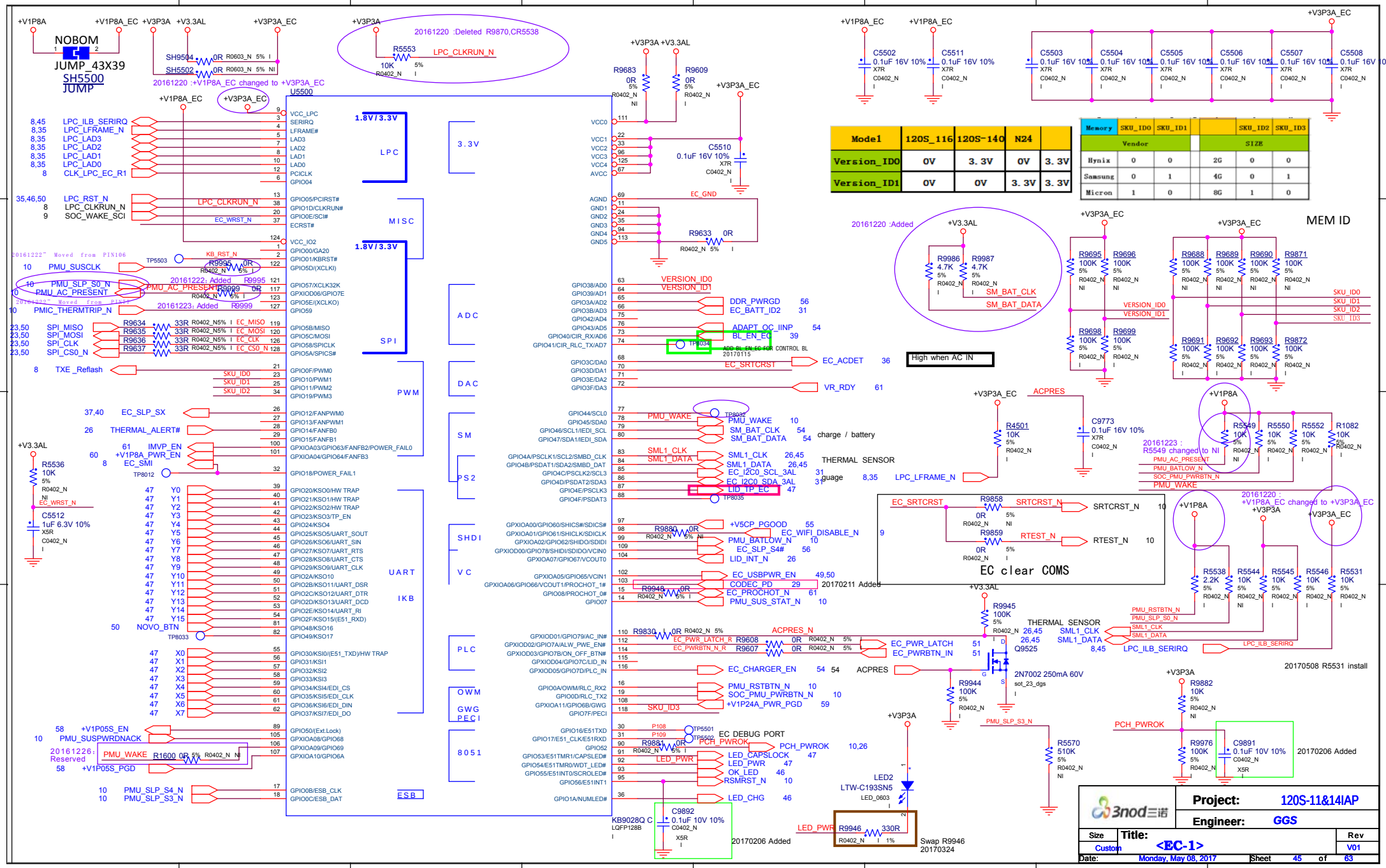
3nod三诺	Project: 120S-11&14IAP	
	Engineer: *LUFFY*	
Size: Custom	Title: <NC>	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 43 of 63	

[PAGE_TITLE=TI PMIC 4 OF 4]

BPAGE DRAWING

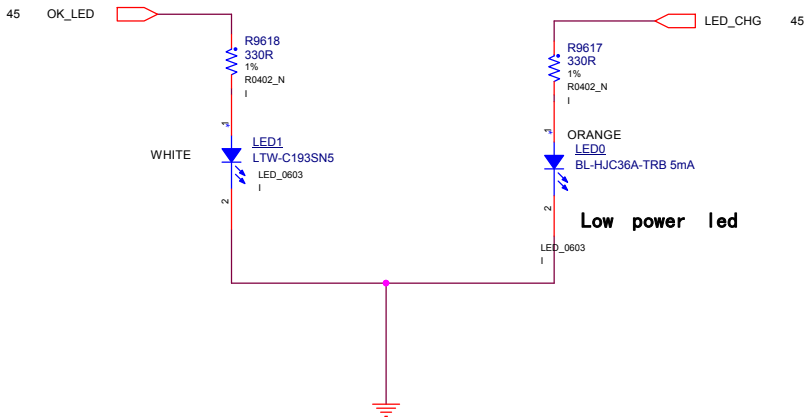
apl_ff.s
Fri May 27 06:47:30 2016

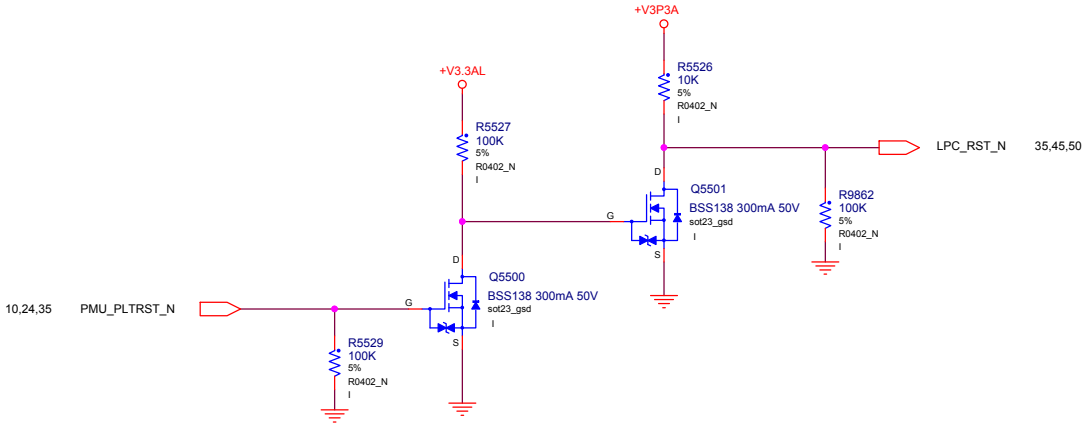
3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: <NC>	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 44 of 63	



Model	120S_116	120S-140	N24	
Version_ID0	0V	3.3V	0V	3.3V
Version_ID1	0V	0V	3.3V	3.3V

Memory	SKU_ID0	SKU_ID1		SKU_ID2	SKU_ID3
Vendor			SIZE		
Hynix	0	0	2G	0	0
Samsung	0	1	4G	0	1
Micron	1	0	8G	1	0



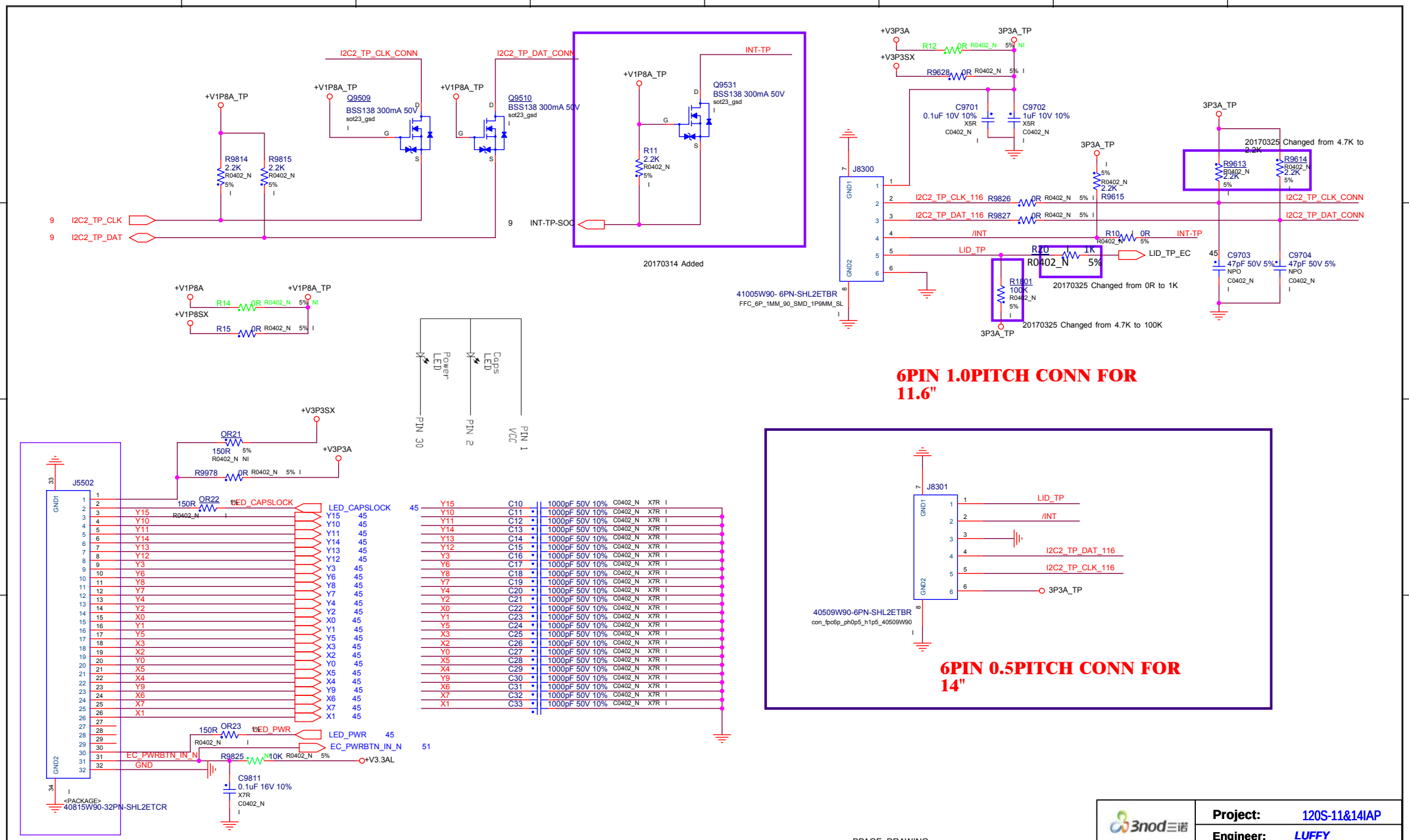


NOTE: CHECK RESET CONNECTION

BPAGE DRAWING

apl_ff.UN$14.141
Fri May 27 06:47:32 2016

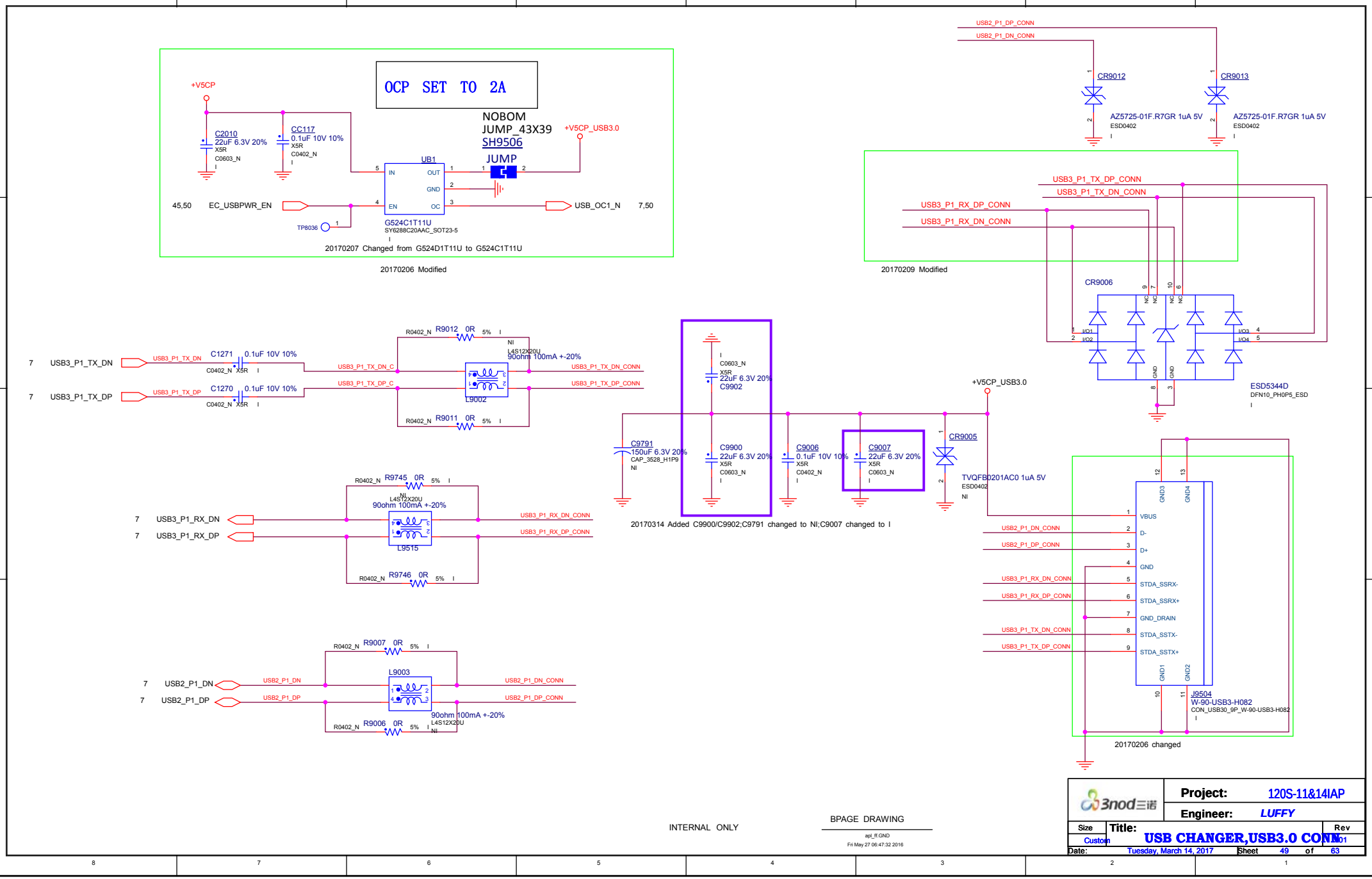
3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: LED AND BUTTON	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 46 of 63	


I2C2_TP_CLK_CONN
I2C2_TP_DAT_CONN
INT-TP
+V1P8A_TP
Q9509
BSS138 300mA 50V
Q9510
BSS138 300mA 50V
Q9531
BSS138 300mA 50V
R9814 2.2K
R9815 2.2K
R11 2.2K
I2C2_TP_CLK
I2C2_TP_DAT
INT-TP-SOC
20170314 Added
+V3P3A
+V3P3SX
3P3A_TP
R12 0R
R9628 0R
C9701 0.1uF 10V 10%
C9702 1uF 10V 10%
J8300
41005W90- 6PN-SHL2ETBR
FFC_6P_1MM_90_SMD_1P9MM_SL
I2C2_TP_CLK_116
I2C2_TP_DAT_116
R9826 0R
R9827 0R
/INT
LID_TP
R9615
R10 0R
LID_TP_EC
R20 1K
R1801 100K
20170325 Changed from 0R to 1K
20170325 Changed from 4.7K to 100K
20170325 Changed from 4.7K to 2.2K
R9613 2.2K
R9614 2.2K
C9703 47pF 50V 5%
C9704 47pF 50V 5%
6PIN 1.0PITCH CONN FOR 11.6"
+V1P8A
+V1P8SX
R14 0R
R15 0R
Power LED
Caps LED
PIN 30
PIN 2
PIN 1
VCC
+V3P3SX
+V3P3A
OR21 150R
R9978 0R
J5502
LED_CAPSLOCK
LED_PWR
EC_PWRBTN_IN_N
GND
OR22 150R
OR23 150R
R9825 10K
+V3.3AL
C9811 0.1uF 16V 10%
40815W90-32PN-SHL2ETCR
20161226:
J5502 PIN SWAP
J8301
40509W90-6PN-SHL2ETBR
con_fpc6p_ph0p5_h1p5_40509W90
6PIN 0.5PITCH CONN FOR 14"
INTERNAL ONLY
BPAGE DRAWING
Project: 120S-11&14IAP
Engineer: LUFFY
Size: Custom
Title: KEY BOARD,TP
Rev: V01
Date: Monday, May 08, 2017
Sheet 47 of 63

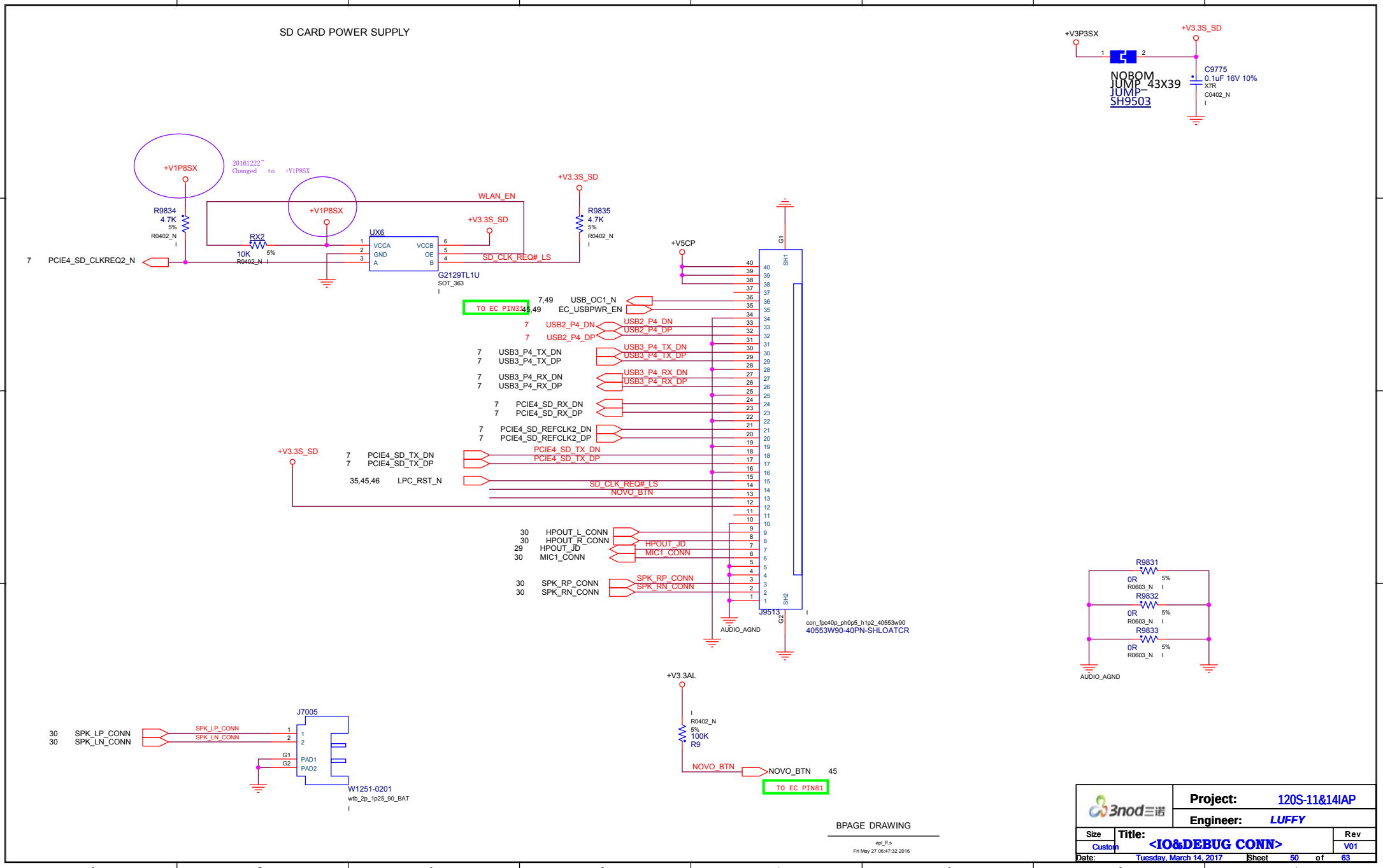
BPAGE DRAWING

apl_ff.GND
Fri May 27 06:47:32 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	*LUFFY*
Size: Custom	Title: <NC>	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 48 of 63	


OCP SET TO 2A
NOBOM
JUMP_43X39
SH9506
JUMP
+V5CP
+V5CP_USB3.0
C2010
22uF 6.3V 20%
X5R
C0603_N
CC117
0.1uF 10V 10%
X5R
C0402_N
UB1
IN
OUT
GND
EN
OC
G524C1T11U
SY6288C20AAC_SOT23-5
45,50
EC_USBPWR_EN
TP8036
USB_OC1_N
7,50
20170207 Changed from G524D1T11U to G524C1T11U
20170206 Modified
USB2_P1_DP_CONN
USB2_P1_DN_CONN
CR9012
CR9013
AZ5725-01F.R7GR 1uA 5V
ESD0402
USB3_P1_TX_DP_CONN
USB3_P1_TX_DN_CONN
USB3_P1_RX_DP_CONN
USB3_P1_RX_DN_CONN
20170209 Modified
CR9006
ESD5344D
DFN10_PH0P5_ESD
7 USB3_P1_TX_DN
7 USB3_P1_TX_DP
USB3_P1_TX_DN
USB3_P1_TX_DP
C1271
C1270
0.1uF 10V 10%
C0402_N
R0402_N
R9012
R9011
0R
5%
NI
L4S12X20U
90ohm 100mA +-20%
USB3_P1_TX_DN_C
USB3_P1_TX_DP_C
USB3_P1_TX_DN_CONN
USB3_P1_TX_DP_CONN
L9002
C0603_N
C9902
22uF 6.3V 20%
C9791
150uF 6.3V 20%
CAP_3528_H1P9
C9900
22uF 6.3V 20%
C9006
0.1uF 10V 10%
C9007
22uF 6.3V 20%
CR9005
TVQFB0201AC0 1uA 5V
ESD0402
20170314 Added C9900/C9902;C9791 changed to NI;C9007 changed to I
7 USB3_P1_RX_DN
7 USB3_P1_RX_DP
R9745
R9746
L9515
7 USB2_P1_DN
7 USB2_P1_DP
USB2_P1_DN
USB2_P1_DP
USB2_P1_DN_CONN
USB2_P1_DP_CONN
R9007
R9006
L9003
VBUS
D-
D+
GND
STDA_SSRX-
STDA_SSRX+
GND_DRAIN
STDA_SSTX-
STDA_SSTX+
GND1
GND2
GND3
GND4
J9504
W-90-USB3-H082
CON_USB30_9P_W-90-USB3-H082
20170206 changed
INTERNAL ONLY
BPAGE DRAWING
apl_ff.GND
Fri May 27 06:47:32 2016
3nod三诺
Project: 120S-11&14IAP
Engineer: LUFFY
Size
Custom
Title: USB CHANGER,USB3.0 CONN
Rev
Date: Tuesday, March 14, 2017
Sheet 49 of 63

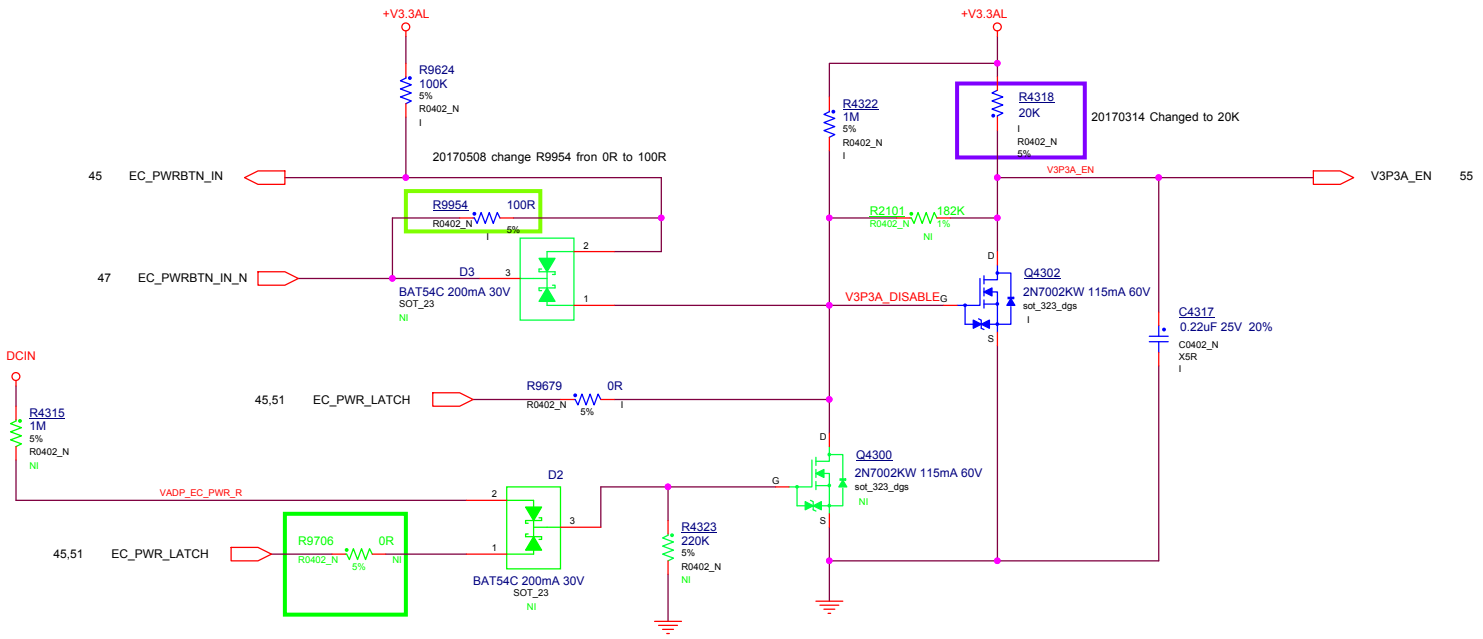
SD CARD POWER SUPPLY



BPAGE DRAWING

apl_ff.s
Fri May 27 06:47:32 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title:	<IO&DEBUG CONN>
		Rev: V01
Date: Tuesday, March 14, 2017	Sheet 50 of 63	



CHANGE TO NI 20170115

BPAGE DRAWING

apl_ff.UN$20.203
Fri May 27 06:47:34 2016

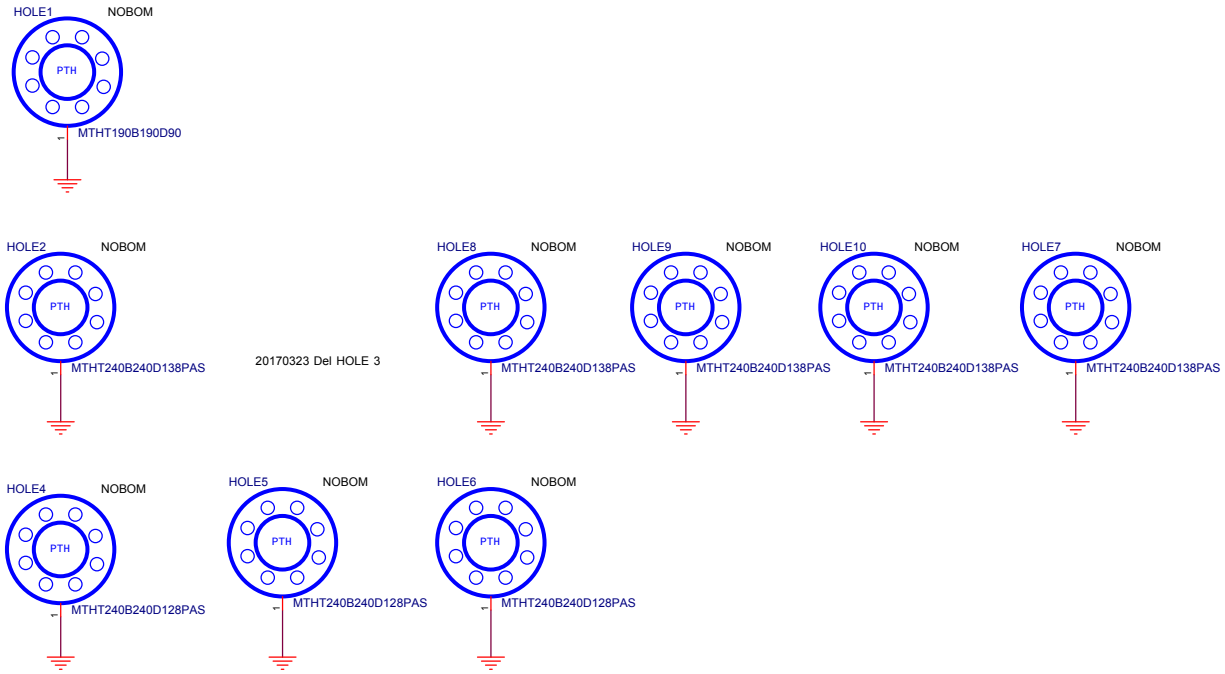
3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: <MISC>	Rev: V01
Date: Monday, May 08, 2017	Sheet 51 of 63	

INTERNAL ONLY

BPAGE DRAWING

apl_ff.UN$20.205
Fri May 27 06:47:34 2016

3nod三诺	Project:	120S-11&14IAP
	Engineer:	LUFFY
Size: Custom	Title: <NC>	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 52 of 63	



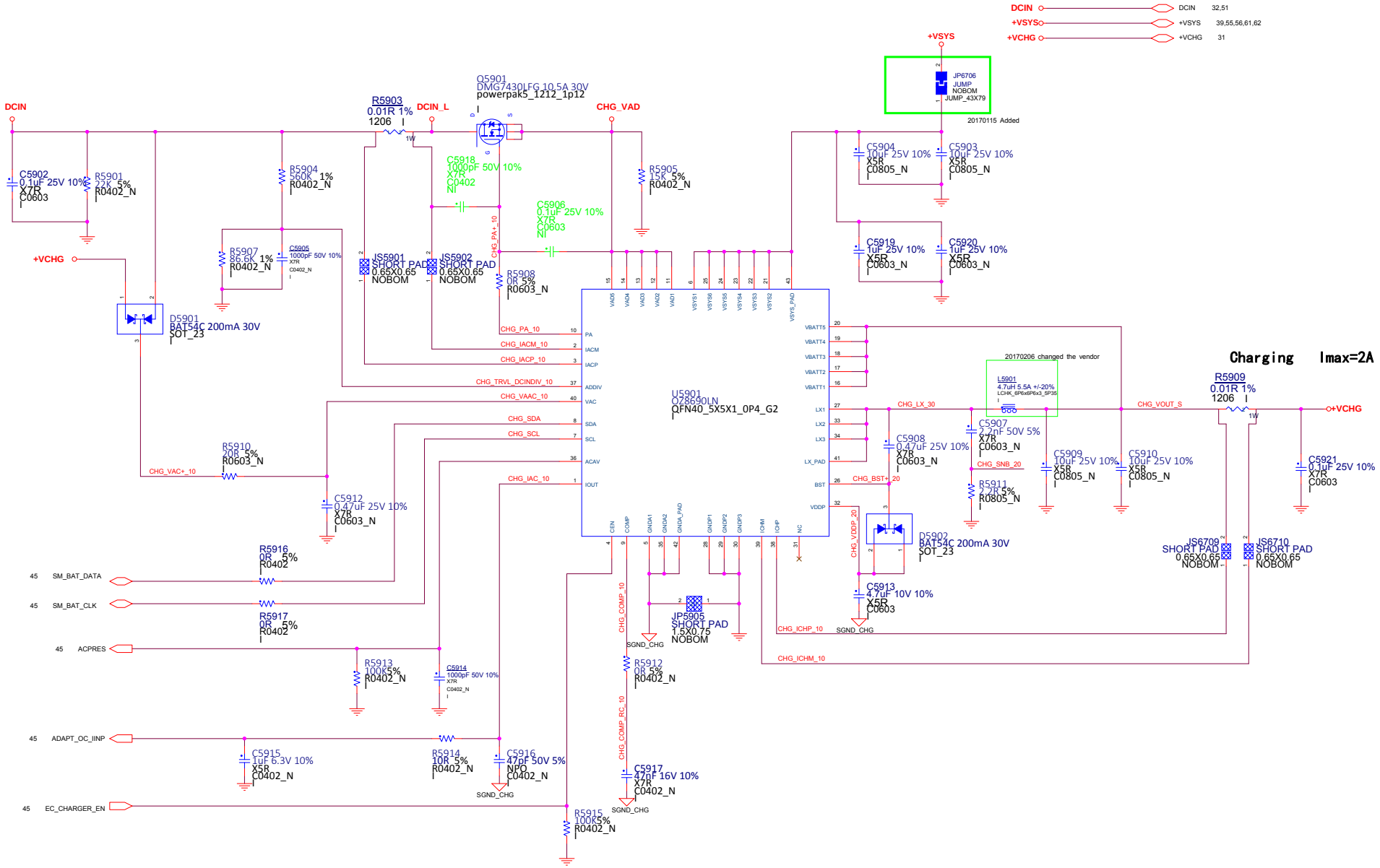
INTERNAL ONLY

BPAGE DRAWING

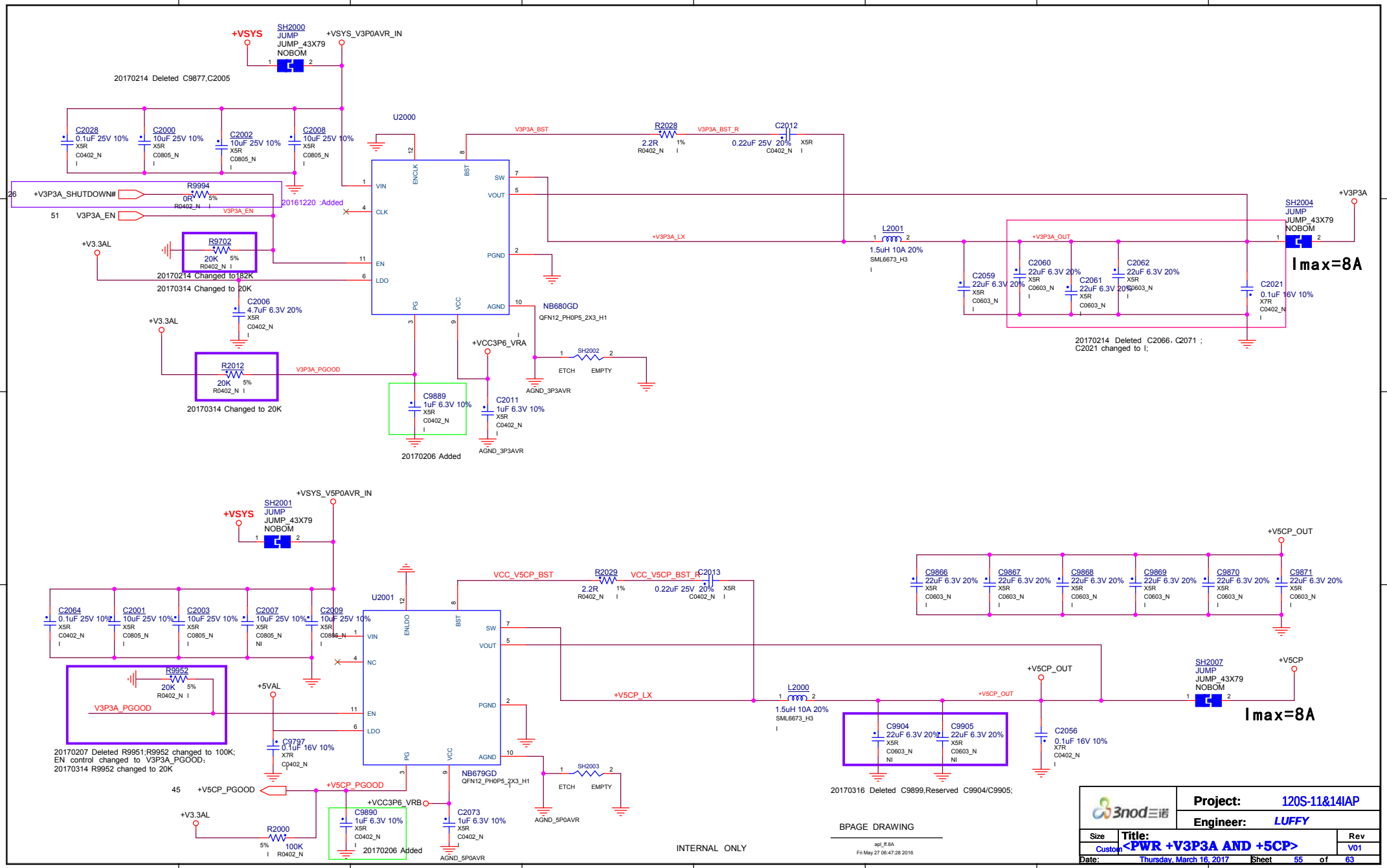
apl_ff.UN$20.205
Fri May 27 06:47:34 2016

3nod三诺	Project: 120S-11&14IAP	
	Engineer: LUFFY	
Size: Custom	Title: <SCREW>	Rev: V01
Date: Friday, March 24, 2017	Sheet 53 of 63	

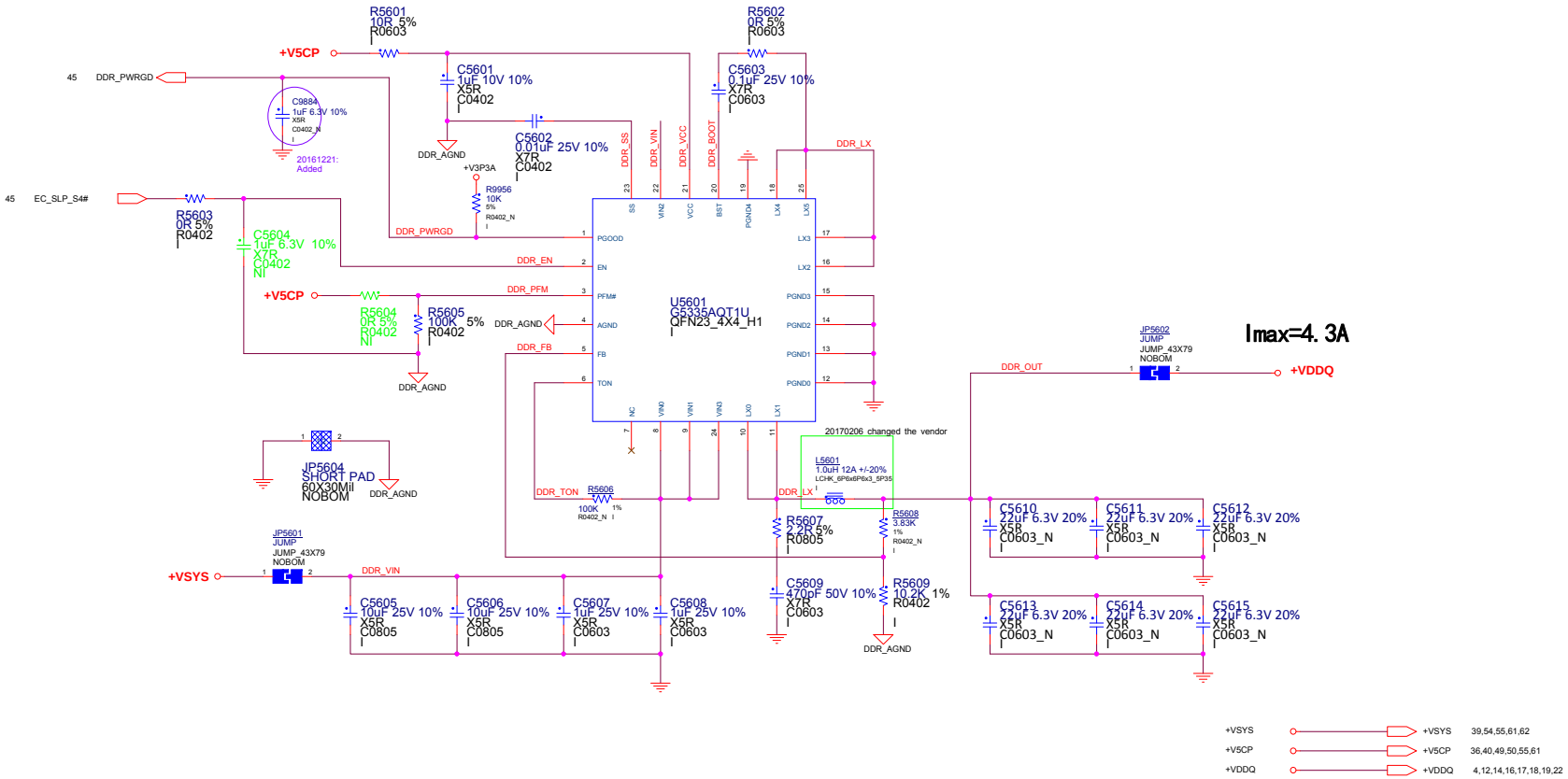
59: BATTERY CHARGER



3nod三诺	Project: 120S-11&14IAP	
	Engineer: Frank	
Size: Custom	Title: <BatteryCharger>	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 54 of 63	


+VSYS
SH2000
JUMP
JUMP_43X79
NOBOM
+VSYS_V3P0AVR_IN
20170214 Deleted C9877,C2005
C2028 0.1uF 25V 10% X5R C0402_N
C2000 10uF 25V 10% X5R C0805_N
C2002 10uF 25V 10% X5R C0805_N
C2008 10uF 25V 10% X5R C0805_N
U2000
V3P3A_BST
R2028 2.2R 1% R0402_N
V3P3A_BST_R
C2012 0.22uF 25V 20% X5R C0402_N
R9994 0R 5% R0402_N
+V3P3A_SHUTDOWN#
V3P3A_EN
20161220 :Added
R9702 20K 5% R0402_N
20170214 Changed to 82K
20170314 Changed to 20K
+V3.3AL
C2006 4.7uF 6.3V 20% X5R C0402_N
R2012 20K 5% R0402_N
V3P3A_PGOOD
20170314 Changed to 20K
C9889 1uF 6.3V 10% X5R C0402_N
20170206 Added
C2011 1uF 6.3V 10% X5R C0402_N
AGND_3P3AVR
+VCC3P6_VRA
NB680GD
QFN12_PH0P5_2X3_H1
SH2002
ETCH
EMPTY
V3P3A_LX
L2001 1.5uH 10A 20% SML6673_H3
V3P3A_OUT
C2059 22uF 6.3V 20% X5R C0603_N
C2060 22uF 6.3V 20% X5R C0603_N
C2061 22uF 6.3V 20% X5R C0603_N
C2062 22uF 6.3V 20% X5R C0603_N
C2021 0.1uF 16V 10% X7R C0402_N
20170214 Deleted C2066、C2071 ; C2021 changed to I;
SH2004
JUMP
JUMP_43X79
NOBOM
+V3P3A
Imax=8A
+VSYS_V5P0AVR_IN
SH2001
JUMP
JUMP_43X79
NOBOM
C2064 0.1uF 25V 10% X5R C0402_N
C2001 10uF 25V 10% X5R C0805_N
C2003 10uF 25V 10% X5R C0805_N
C2007 10uF 25V 10% X5R C0805_N
C2009 10uF 25V 10% X5R C0805_N
U2001
VCC_V5CP_BST
R2029 2.2R 1% R0402_N
VCC_V5CP_BST_R
C2013 0.22uF 25V 20% X5R C0402_N
R9952 20K 5% R0402_N
V3P3A_PGOOD
+5VAL
C9797 0.1uF 16V 10% X7R C0402_N
20170207 Deleted R9951;R9952 changed to 100K;
EN control changed to V3P3A_PGOOD;
20170314 R9952 changed to 20K
NB679GD
QFN12_PH0P5_2X3_H1
SH2003
ETCH
EMPTY
AGND_5P0AVR
+V5CP_PGOOD
45 +V5CP_PGOOD
+V3.3AL
R2000 100K 5% R0402_N
+VCC3P6_VRB
C9890 1uF 6.3V 10% X5R C0402_N
20170206 Added
C2073 1uF 6.3V 10% X5R C0402_N
AGND_5P0AVR
+V5CP_LX
L2000 1.5uH 10A 20% SML6673_H3
C9904 22uF 6.3V 20% X5R C0603_N NI
C9905 22uF 6.3V 20% X5R C0603_N NI
20170316 Deleted C9899,Reserved C9904/C9905;
C9866 22uF 6.3V 20% X5R C0603_N
C9867 22uF 6.3V 20% X5R C0603_N
C9868 22uF 6.3V 20% X5R C0603_N
C9869 22uF 6.3V 20% X5R C0603_N
C9870 22uF 6.3V 20% X5R C0603_N
C9871 22uF 6.3V 20% X5R C0603_N
+V5CP_OUT
C2056 0.1uF 16V 10% X7R C0402_N
SH2007
JUMP
JUMP_43X79
NOBOM
+V5CP
Imax=8A
INTERNAL ONLY
BPAGE DRAWING
apl_IE8A
Fri May 27 06:47:28 2016
Project: 120S-11&14IAP
Engineer: LUFFY
Size: Custom
Title: <PWR +V3P3A AND +5CP>
Rev: V01
Date: Thursday, March 16, 2017
Sheet 55 of 63

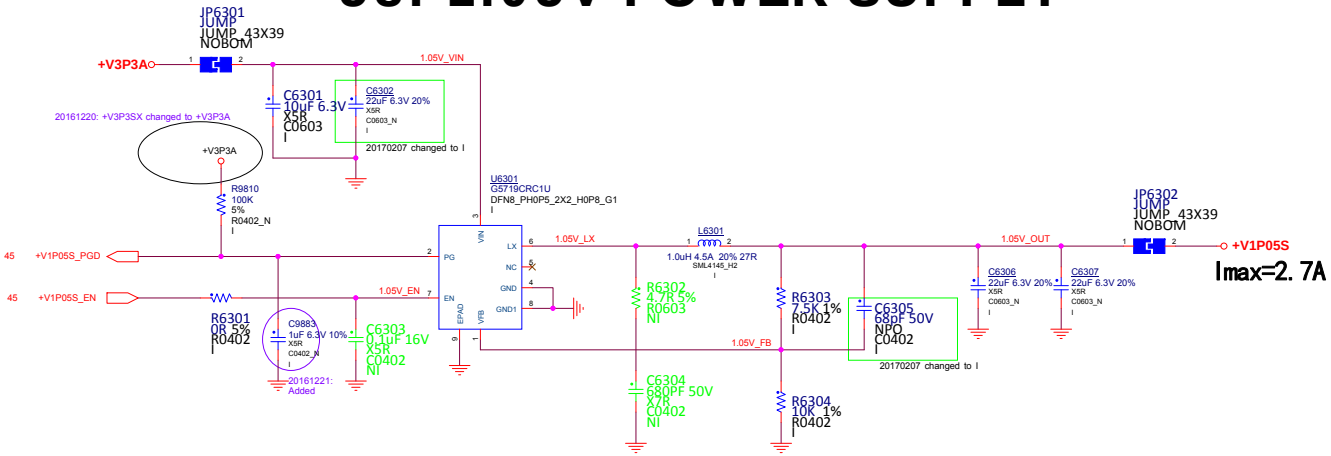
56: DDR POWER SUPPLY



3nod三诺	Project: 120S-11&14IAP	
	Engineer: Frank	
Size C	Title: <DDR Power>	Rev V01
Date: Tuesday, March 14, 2017	Sheet 56 of 63	

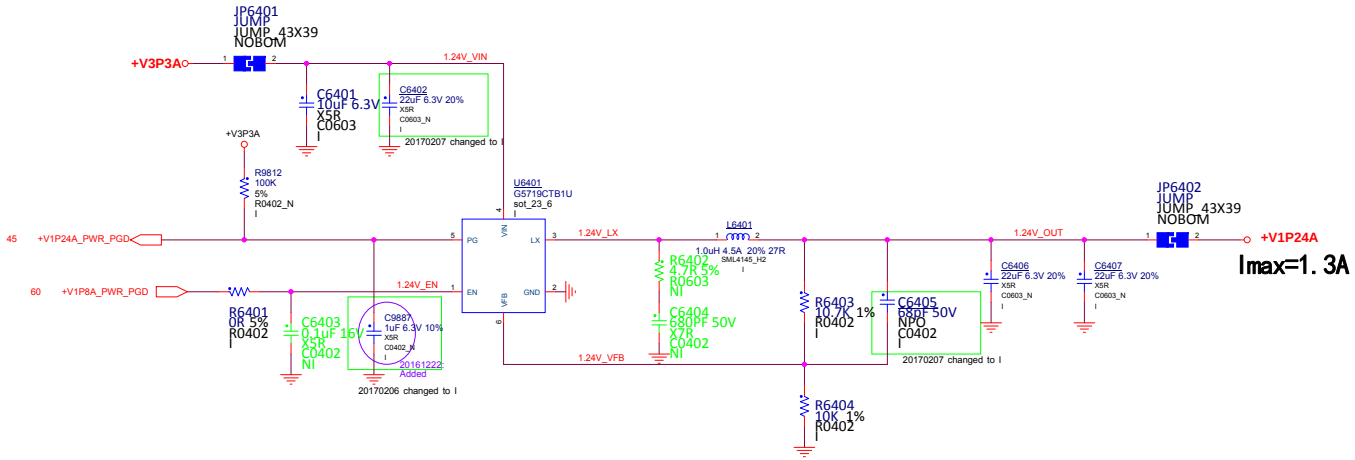
3nod三诺	Project: 120S-11&14IAP	
	Engineer: Frank	
Size C	Title: <NC>	Rev V01
Date: Tuesday, March 14, 2017	Sheet 57 of 63	

58: 1.05V POWER SUPPLY



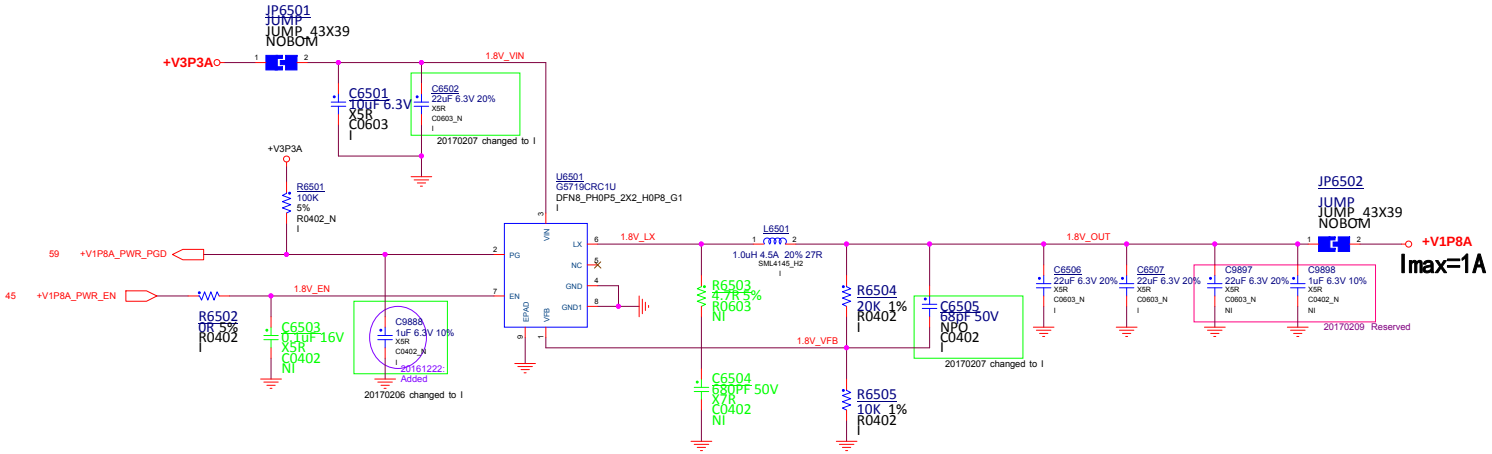
3nod三诺	Project: 120S-11&14IAP	
	Engineer: Frank	
Size C	Title: <1.05V POWER SUPPLY>	Rev V01
Date: Tuesday, March 14, 2017	Sheet 58 of 63	

59: 1.24V POWER SUPPLY



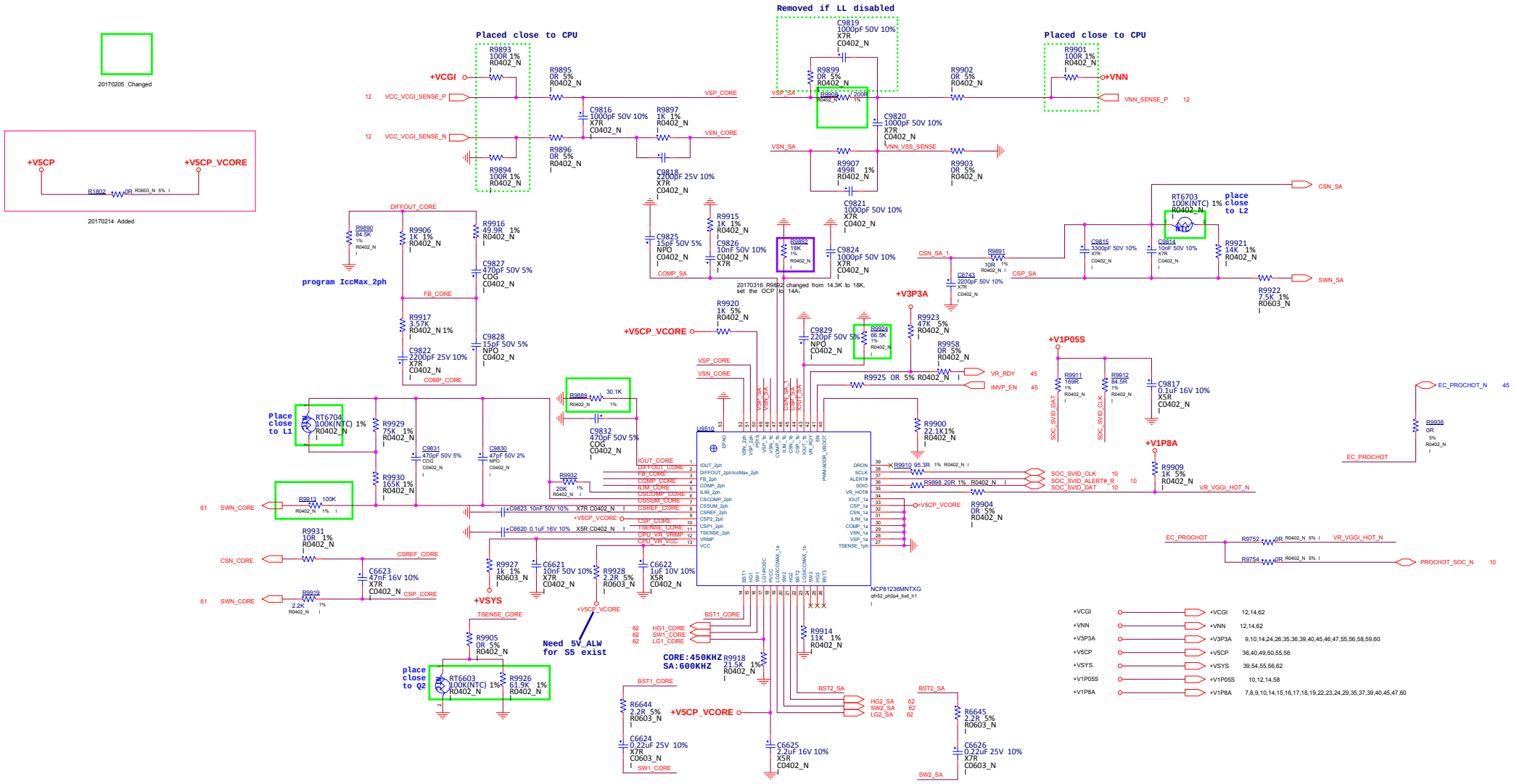
3nod三诺	Project: 120S-11&14IAP	
	Engineer: Frank	
Size C	Title: <1.24V POWER SUPPLY>	Rev V01
Date: Tuesday, March 14, 2017	Sheet 59 of 63	

60: +1.8V POWER SUPPLY



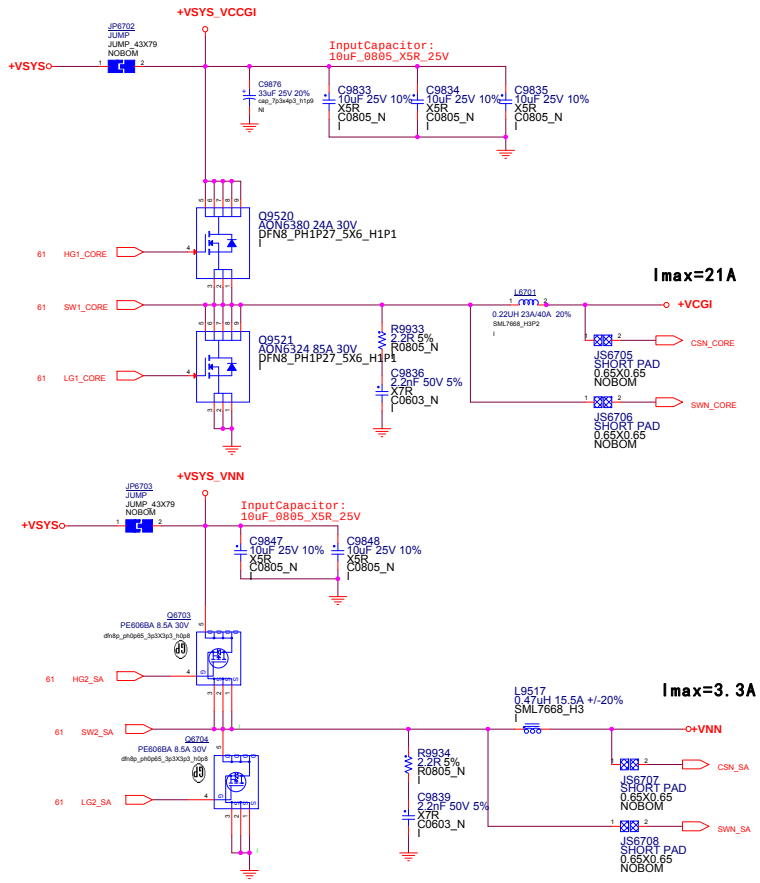
3nod三诺	Project: 120S-11&14IAP	
	Engineer: Frank	
Size: C	Title: <+1.8V_PRIM>	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 60 of 63	

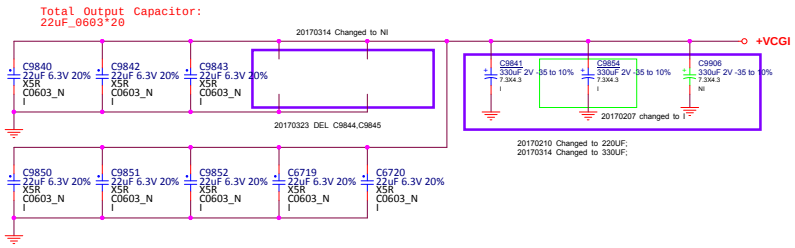
CPU POWER SUPPLY

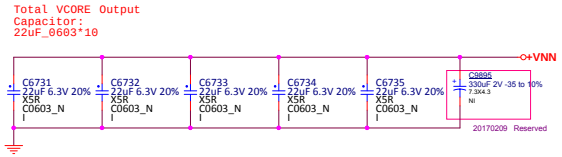


3nod三诺	Project: NA	
	Engineer: Frank	
Size	Title: <VCGI AND VNN_1>	Rev
Custom		V01
Date: Thursday, March 16, 2017	Sheet 61 of 63	

VCGI / VNN POWER SUPPLY



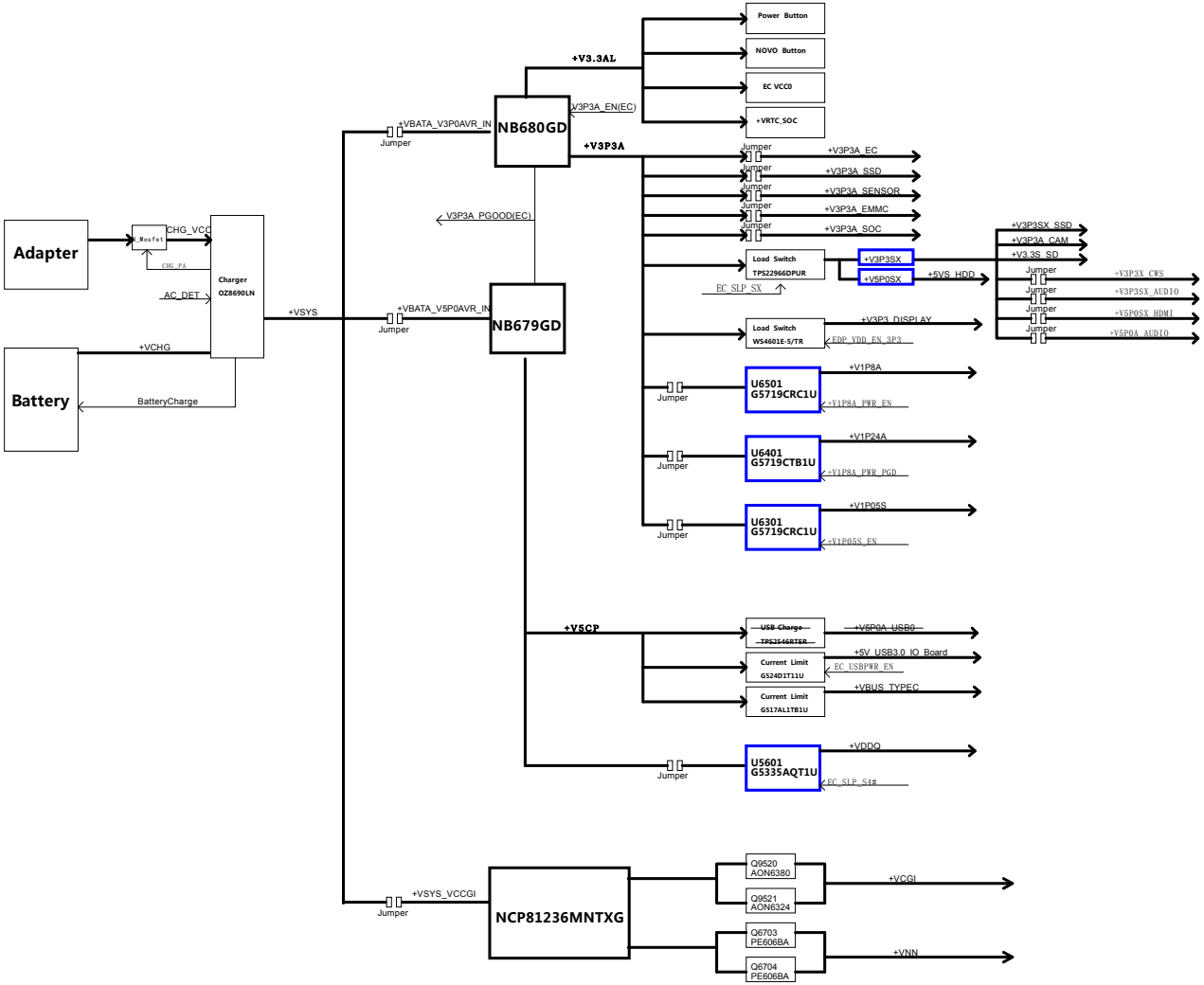




+VCGI	+VCGI	12,14,61
+VNN	+VNN	12,14,61
+VSYS	+VSYS	39,54,55,56,61

3nod三诺	Project: NA	
	Engineer: Frank	
Size: Custom	Title: <VCGI AND VNN_2>	Rev: V01
Date: Thursday, March 23, 2017	Sheet 62 of 63	

Apollo Lake Platform Power Map



3nod三诺	Project: 120S-11&14IAP	
	Engineer: Frank	
Size: C	Title: <PWR BLOCK DIAGRAM>	Rev: V01
Date: Tuesday, March 14, 2017	Sheet 63 of 63	