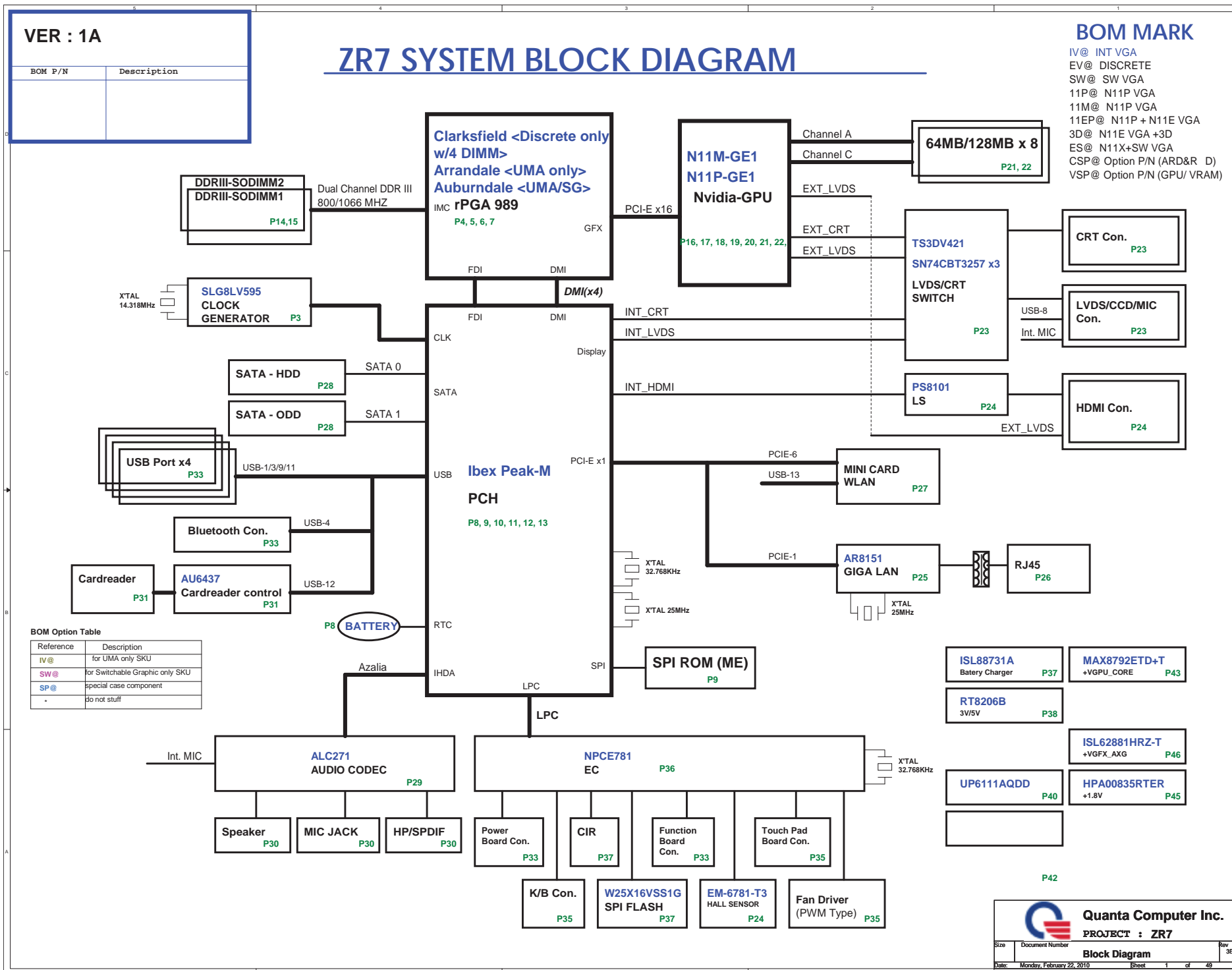


VER : 1A

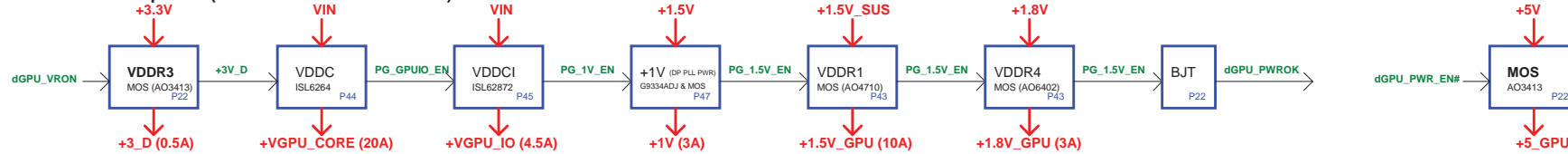
# ZR7 SYSTEM BLOCK DIAGRAM

## BOM MARK

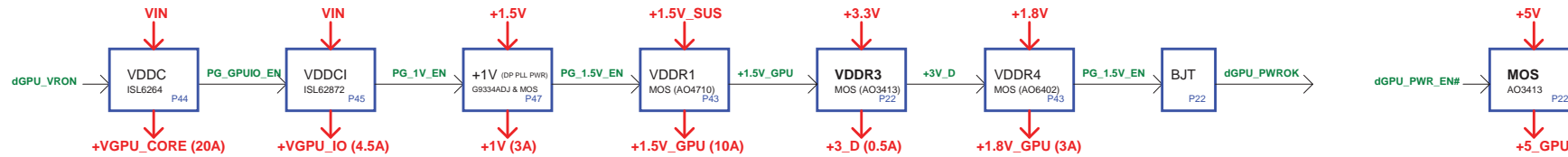
IV@ INT VGA  
EV@ DISCRETE  
SW@ SW VGA  
11P@ N11P VGA  
11M@ N11P VGA  
11EP@ N11P + N11E VGA  
3D@ N11E VGA +3D  
ES@ N11X+SW VGA  
CSP@ Option P/N (ARD&R D)  
VSP@ Option P/N (GPU/ VRAM)



### GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



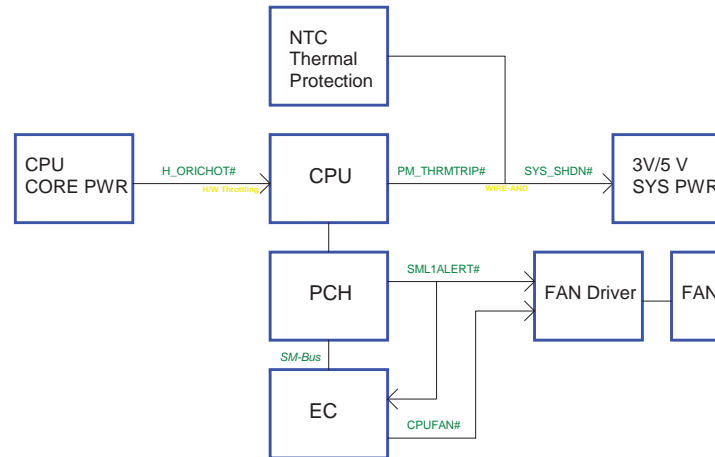
### GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



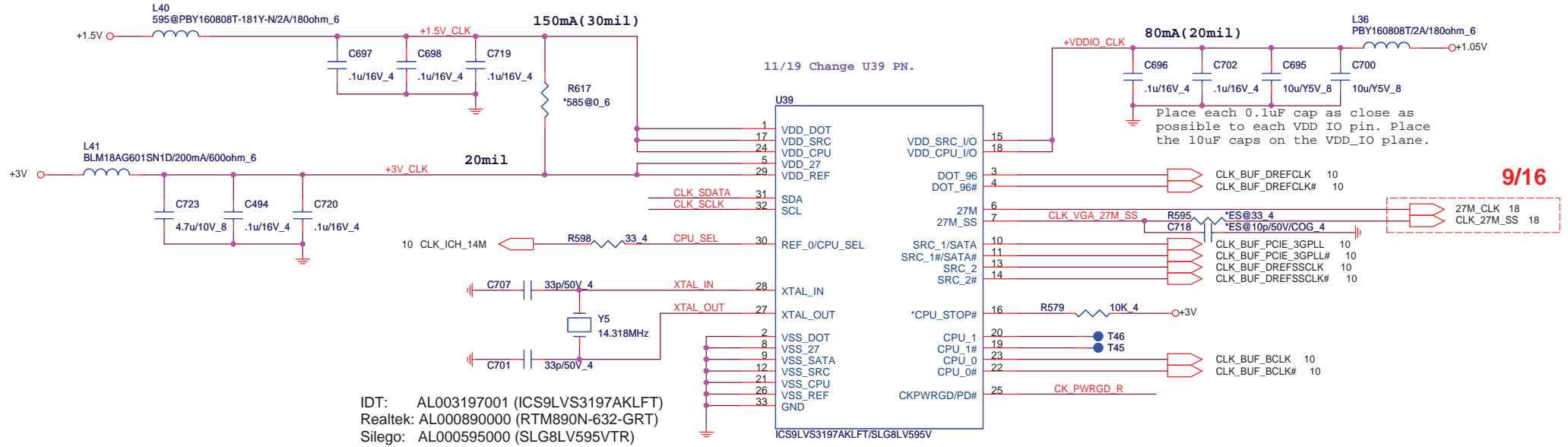
### Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BIOS/PCI POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

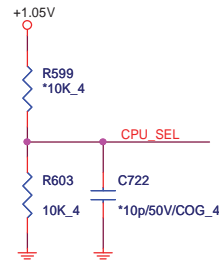
### Thermal Follow Chart



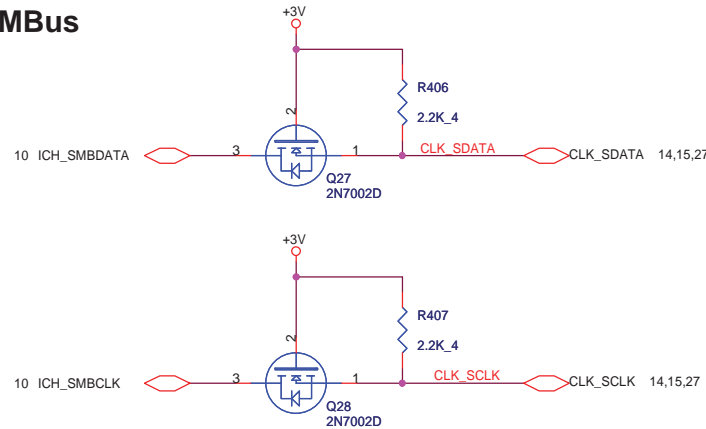
## CLK GEN.



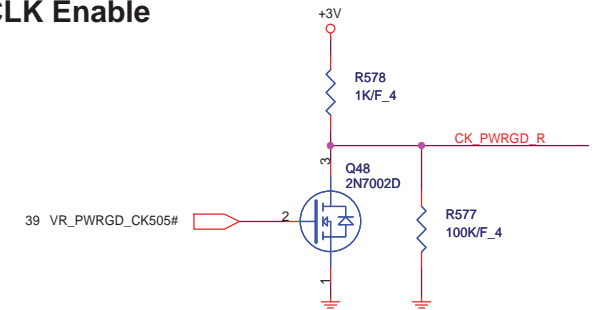
## CPU\_CLK select



## SMBus



## CLK Enable



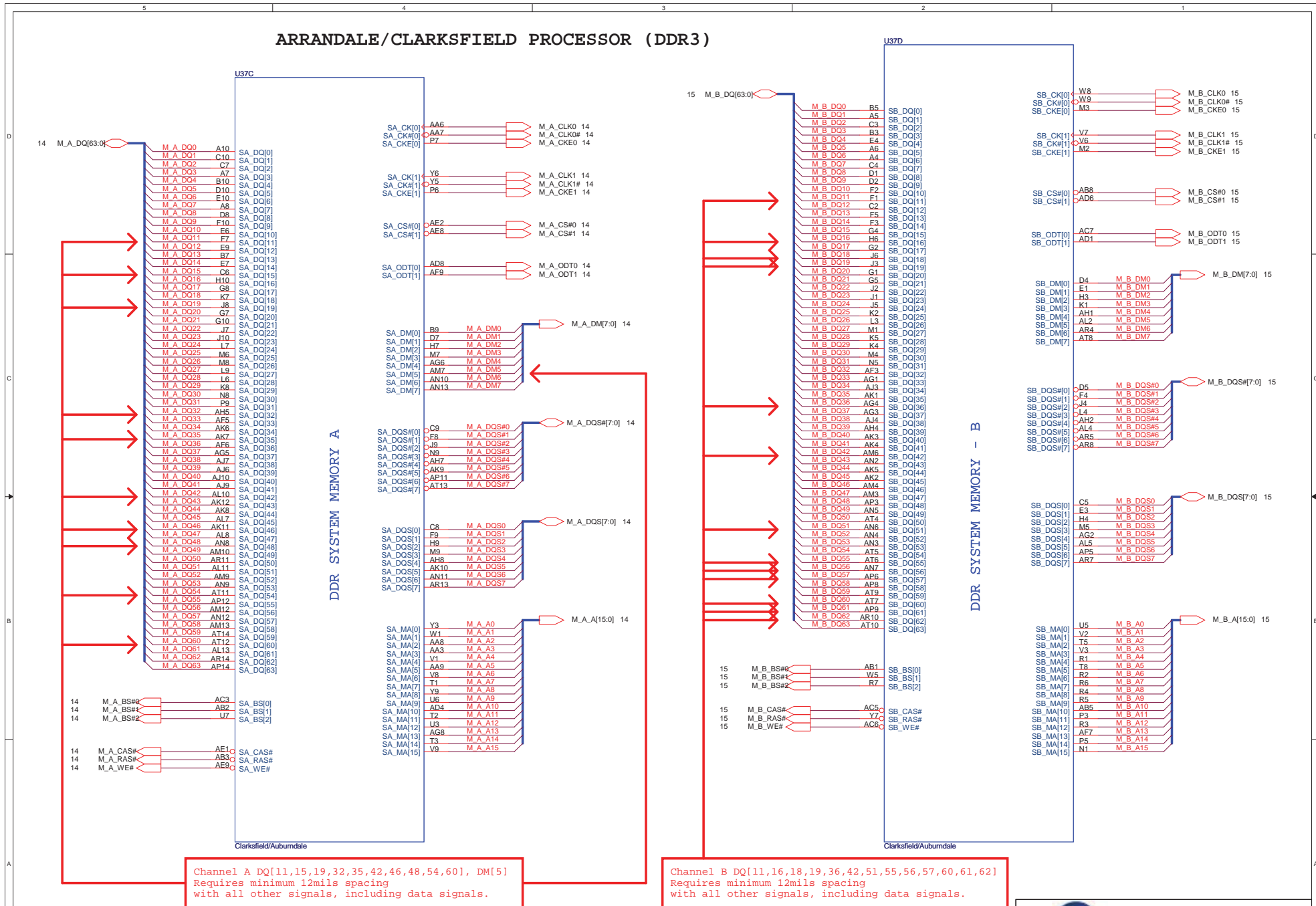
**Quanta Computer Inc.**

**PROJECT : ZR7**

Size	Document Number	Rev
	<b>Clock Generator</b>	<b>3B</b>
Date:	Monday, February 22, 2010	Sheet 3 of 49

ARRANDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)

## ARRANDALE/CLARKSFIELD PROCESSOR (DDR3)



**Quanta Computer Inc.**  
**PROJECT : ZR7**

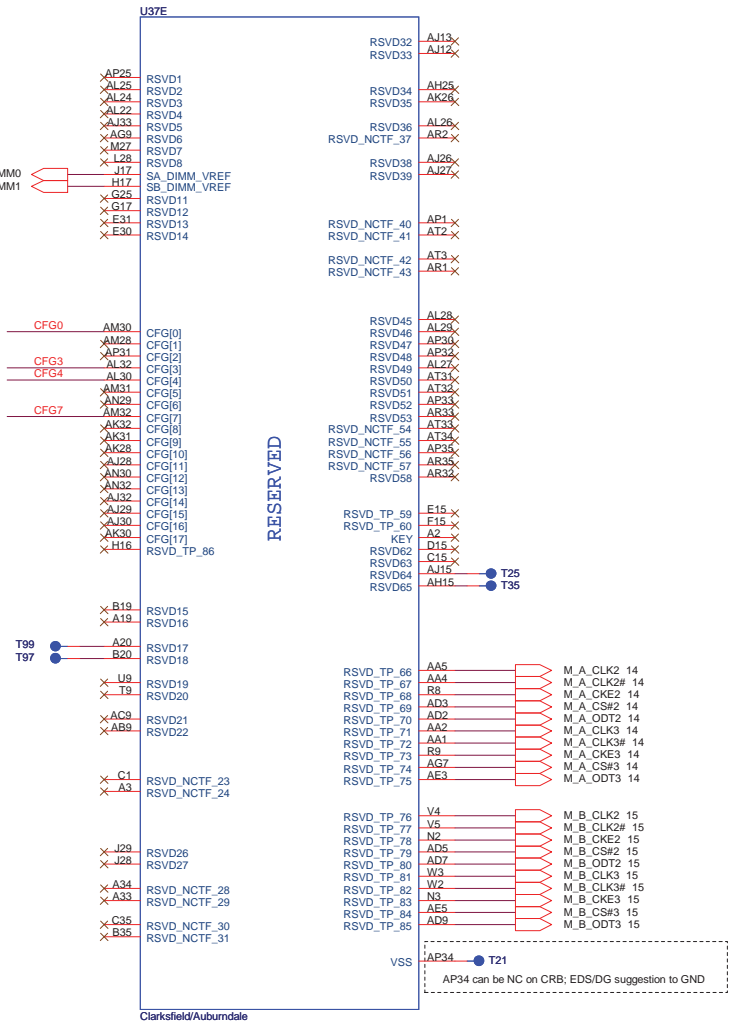
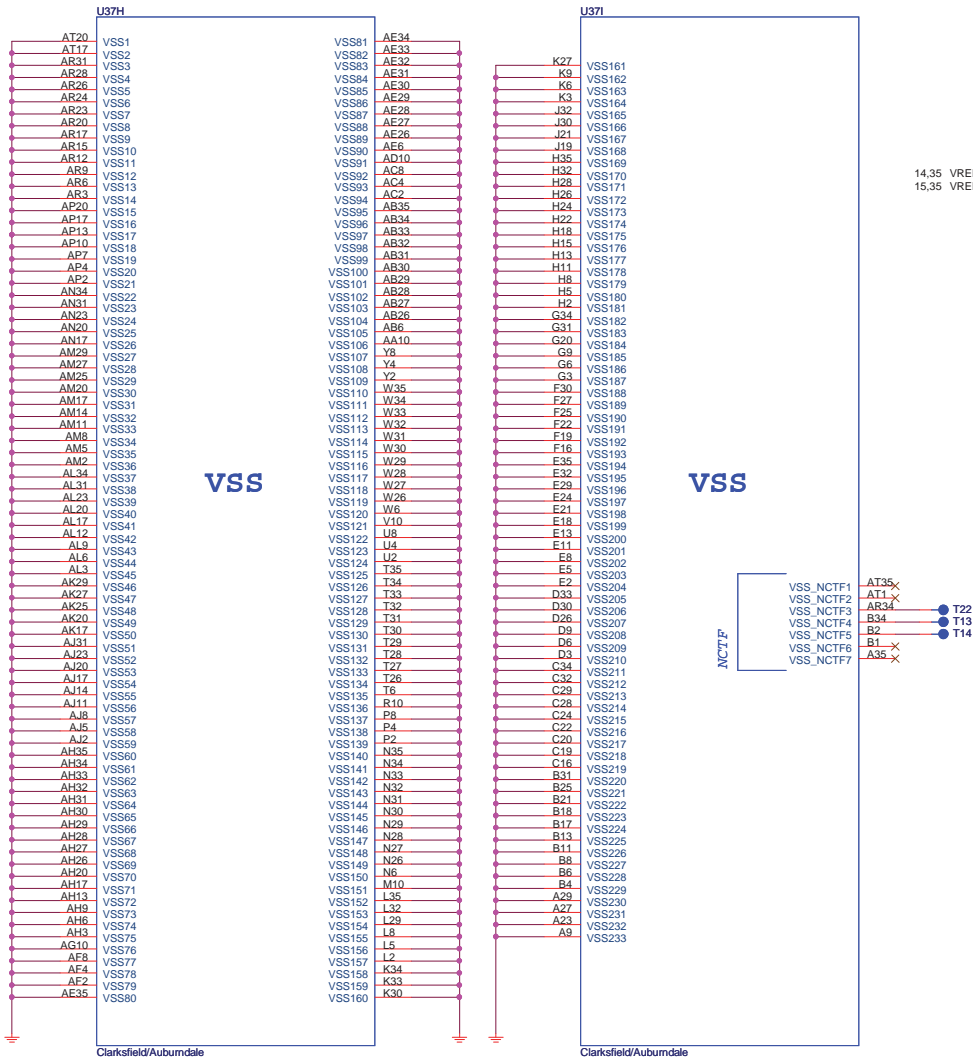
Size	Document Number	Rev
	<b>ARRANDALE/CLARKSFIELD 2/4</b>	3B
Date:	Monday, February 22, 2010	Sheet 5 of 49





# ARRANDALE/CLARKSFIELD PROCESSOR (GND)

# ARRANDALE/CLARKSFIELD PROCESSOR( RESERVED, CFG)

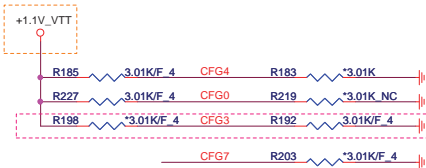


## Processor Strapping

	1	0	DEFAULT
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled	1
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed	1
CFG4 (Embedded Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port	1
The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.			

VTT Rail Values are  
Arrandale VTT=1.05V  
Clarksville VTT=1.1V

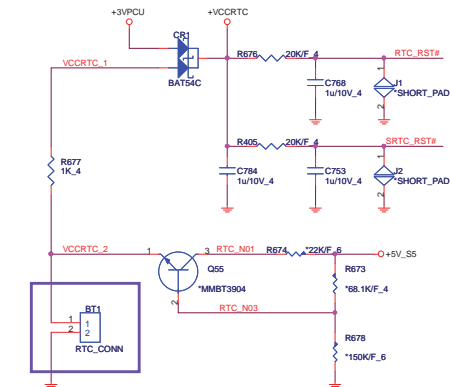
Use reverse type





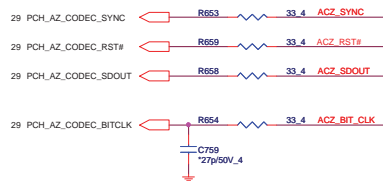


## RTC Circuitry



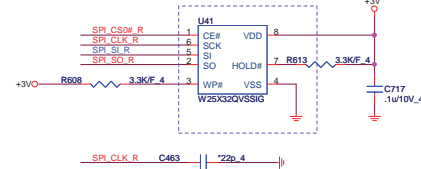
1/7 Change P/N by ME.

## HDA Bus

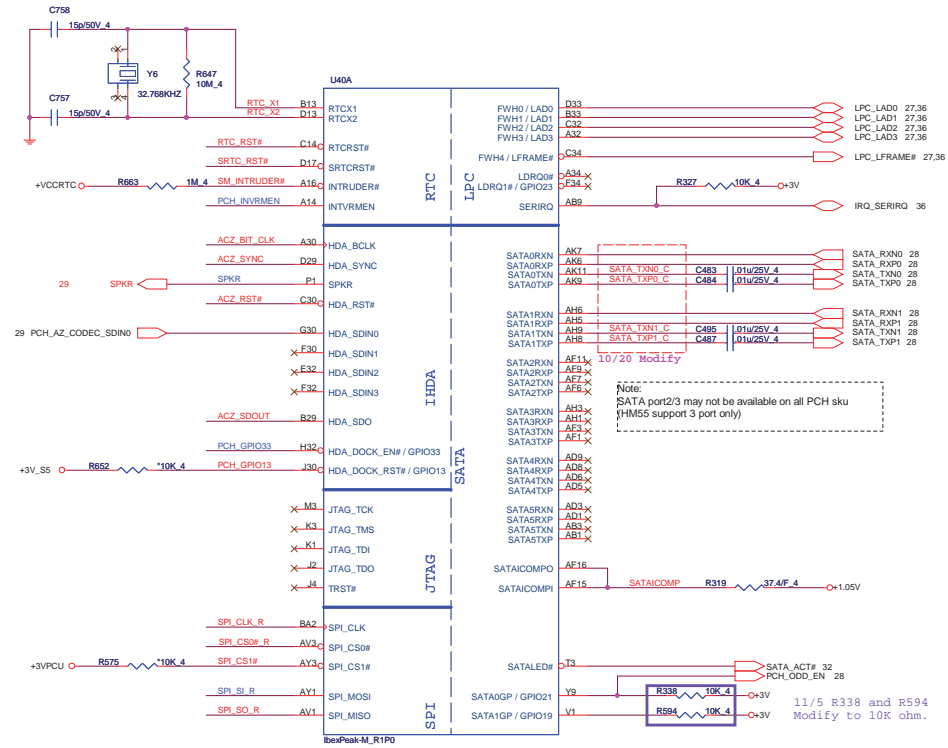


## PCH SPI

10/29 Modify P/N to 2M  
12/7 Modify P/N to 4M



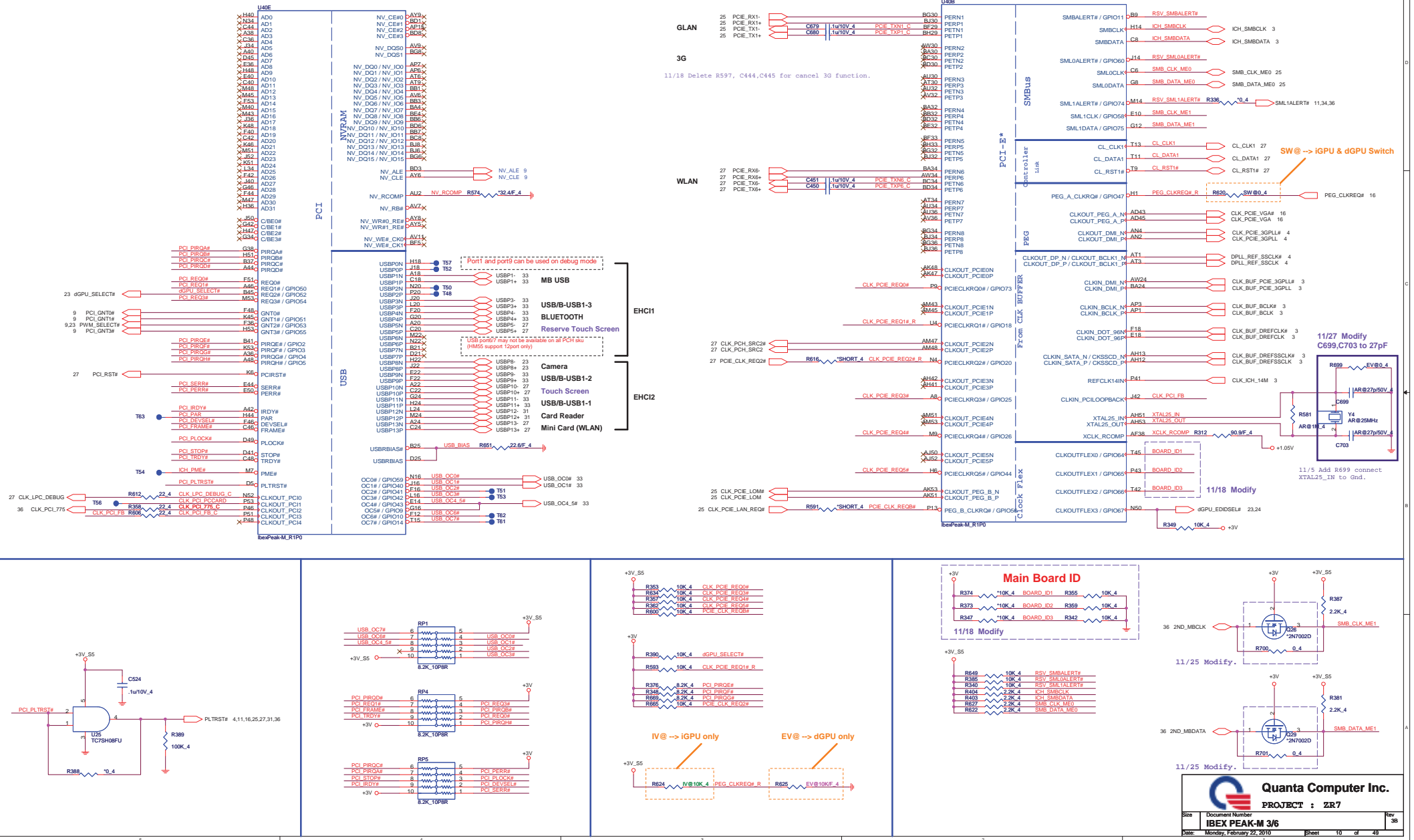
**HDA\_SYNC (PCH strap pin)**  
Internal weak pull-down  
VCCVRM=>+1.8V (default)  
external pull-up  
VCCVRM=>+1.5V



PCH Strap Pin Configuration Table-1

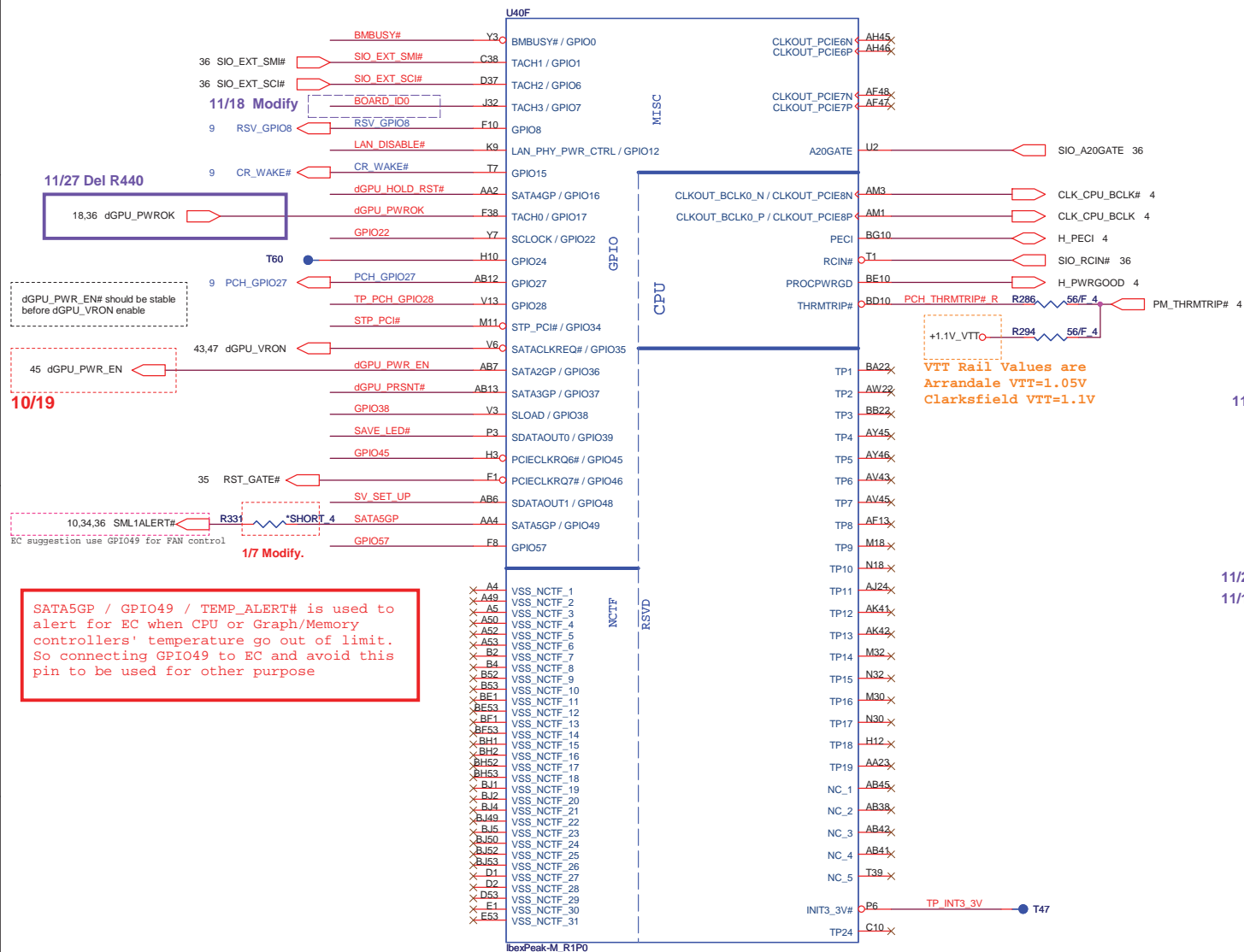
INTVRMEN	Integrated 1.05V VRM Enable / Disable	1 = Integrated VRM is enabled 0 = Integrated VRM is disabled	+VCCRTC ○ R695 330K_6 PCH_INVRMEN
SPI_MOSI	TPM Functionality Disable	1 = Enabled 0 = Disabled	+3V ○ R618 1K_4 SPI_SI_R
SPKR	Reboot option at power-up	0 = Default Mode (Internal weak Pull-down) 1 = No Reboot Mode with TCO Disabled	+3V ○ R611 1K/4_4SPKR
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Override	0 = Flash Descriptor Security will be overridden 1 = Security measure defined in the Flash Descriptor will be enabled.	PCH_GPIO33 R370 1K/4_4 R365 10K_4 +3V
GNT0#, GNT1#	Boot BIOS Strap	(0,0) = LPC (0,1) = Reserved NAND (1,0) = PCI (1,1) = SPI	PCH_GNT0# R360 1K_4 PCH_GNT1# R363 1K_4
GNT2#/GPIO53	ESI Strap (Server Only)	ESI compatible mode is for server platforms only	10,23 PWM_SELECT# R364 1K/4_4
GNT3#/GPIO55	Top-Block Swap Override	0 = Top Block Swap Mode 1 = Default Mode (Internal pull-up)	10 PCH_GNT3# R628 10K/4_4
NV_ALE	Intel® Anti-Theft Technology HDD Data Protection (Intel AT-D) Enable	1 = Enabled 0 = Disabled (Default)	10 NV_ALE R296 1K/4_4 +1.8V
NV_CLE	DMI Termination Voltage	DMI termination voltage. Weak internal pull-up. Do not pull low.	10 NV_CLE R295 1K/4_4 +1.8V
GPIO8	Reserved	This signal has a weak internal pull up. NOTE: This signal should not be pulled low	11 RSV_GPIO8 R380 10K_4 +3V_S5 R371 1K_4
GPIO15	Reserved	0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality	11 CR_WAKE# R341 1K_4 +3V_S5
GPIO27	On-Die PLL Voltage Regulator <internal weak pull-up>	0 = Disables the VccVRM. 1 = Enables the internal VccVRM to have a clean supply for analog rails.	11 PCH_GPIO27 R324 10K_4

IV@ --> iGPU only  
EV@ --> dGPU only  
SW@ --> iGPU & dGPU Switch

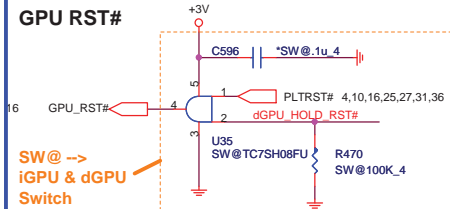


IV@ --> iGPU only  
EV@ --> dGPU only  
SW@ --> iGPU & dGPU Switch  
ES@ --> External VGA SKU

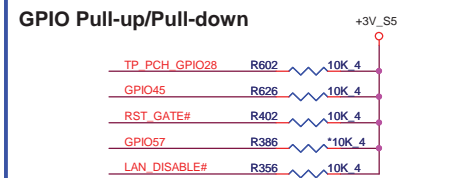
## IBEX PEAK-M (GPIO,VSS\_NCTF,RSVD)



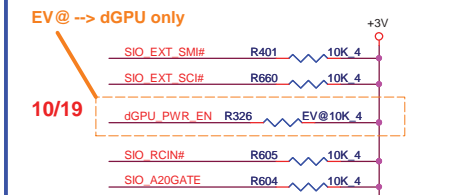
## GPU RST#



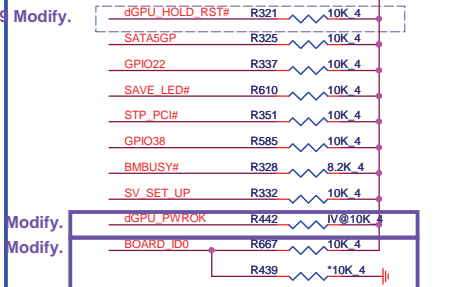
## GPIO Pull-up/Pull-down



EV @ --> dGPU only

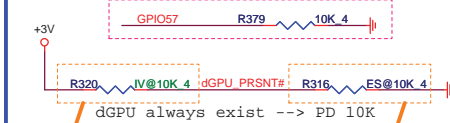


### 9 Modify.



SV_SET_UP	1-X High = Strong (Default)
-----------	-----------------------------

GPI057 stuff PD and not stuff PU for Intel suggestion at 6/1



IV@ --> iGPU only

ES@ --> External VGA SKU

Integrated Clock Chip Enable	
RSV_GPIO8	High = Disable Low = Enable



**Quanta Computer Inc.**

PROJECT : ZR7

# IBEX PEAK-M (POWER)

AR@ -> ARD CPU  
CF@ -> CFD CPU

VCCCORE(+1.05V) = 1.432A(80mils)

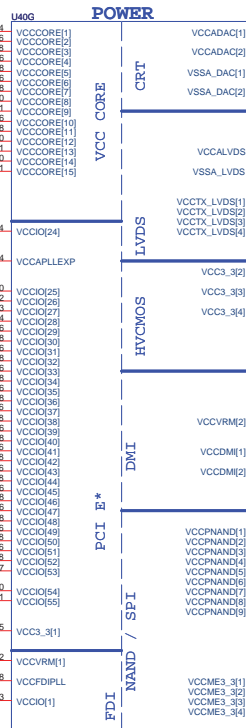
40mA(15mils)

VCCIO = 3.062A(150mils)

37mA(15mils)

VRM enable by strap pin GPIO27  
which supply clean 1.05V for  
[VCCACLK, VCCAPLLEXP, VCCFDIPLL, VCCSATAPLL]

## POWER



IbexPeak-M\_R1P0

VCCVRM=196mA(15mils)

VCCVRM=196mA(15mils)

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VCCVRM=196mA(15mils)

HDA\_SYNC (PCH strap pin)  
Internal weak pull-down  
VCCVRM=>+1.8V (default)  
external pull-up  
VCCVRM=>+1.5V

VTT Rail Values are  
Arrandale VTT=1.05V  
Clarksfield VTT=1.1V

VCCSUS3\_3 = 163mA(20mils)

VCC3\_3 = 0.357A(30mils)

V\_CPU\_IO > 1mA(15mils)

VCCRTC = 2mA(15mils)

VCCSUS3\_3 = 163mA(20mils)

VCC3\_3 = 0.357A(30mils)

V\_CPU\_IO > 1mA(15mils)

VCCRTC = 2mA(15mils)

VCCSUS3\_3 = 163mA(20mils)

VCC3\_3 = 0.357A(30mils)

V\_CPU\_IO > 1mA(15mils)

AR@ -> ARD CPU  
CF@ -> CFD CPU

VCCACLK = 52mA(15mils)

VCCALVDS = 1mA

VCC3\_3 = 357mA(30mils)

VCCVRM = 196mA(15mils)

VCCVPM = 196mA(15mils)

VCCPNAND = 156mA(15mils)

VCCVRM = 196mA(15mils)

VCCVRM = 196mA(15mils)

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## POWER

VCCIO = 3.208A(150mils)

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VCCIO = 3.208A(150mils)

VCCADAC = 69mA(15mils)

VCCALVDS = 1mA

VCC3\_3 = 357mA(30mils)

VCCVRM = 196mA(15mils)

VCCVPM = 196mA(15mils)

VCCPNAND = 156mA(15mils)

VCCVRM = 196mA(15mils)

VCCVRM = 196mA(15mils)

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VCCVRM = 196mA(15mils)

VCCVRM = 196mA(15mils)

VCCADAC = 69mA(15mils)

VCCALVDS = 1mA

VCC3\_3 = 357mA(30mils)

VCCVRM = 196mA(15mils)

VCCVPM = 196mA(15mils)

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VCCVRM = 196mA(15mils)

VCCVRM = 196mA(15mils)

VCCVRM = 196mA(15mils)

VCCADAC = 69mA(15mils)

VCCALVDS = 1mA

VCC3\_3 = 357mA(30mils)

VCCVRM = 196mA(15mils)

VCCVPM = 196mA(15mils)

VCCPNAND = 156mA(15mils)

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VCCVRM = 196mA(15mils)

VCCVRM = 196mA(15mils)

VCCVRM = 196mA(15mils)

VCCADAC = 69mA(15mils)

VCCALVDS = 1mA

VCC3\_3 = 357mA(30mils)

VCCVRM = 196mA(15mils)

VCCVPM = 196mA(15mils)

VCCPNAND = 156mA(15mils)

# IBEX PEAK-M (GND)

U40H


AB16	VSS[0]	
AA19	VSS[1]	VSS[80] AK30
AA20	VSS[2]	VSS[81] AK31
AA22	VSS[3]	VSS[82] AK32
AM19	VSS[4]	VSS[83] AK33
AA24	VSS[5]	VSS[84] AK34
AA26	VSS[6]	VSS[85] AK35
AA28	VSS[7]	VSS[86] AK36
AA30	VSS[8]	VSS[87] AK37
AA31	VSS[9]	VSS[88] AK38
AA32	VSS[10]	VSS[89] AK39
AB11	VSS[11]	VSS[90] AK40
AB15	VSS[12]	VSS[91] AL2
AB23	VSS[13]	VSS[92] AM11
AB31	VSS[14]	VSS[93] BB44
AB32	VSS[15]	VSS[94] AD24
AB39	VSS[16]	VSS[95] AM20
AB43	VSS[17]	VSS[96] AM22
AB47	VSS[18]	VSS[97] AM24
AB5	VSS[19]	VSS[98] AM26
AB8	VSS[20]	VSS[99] AM28
AC2	VSS[21]	VSS[100] RA42
AC32	VSS[22]	VSS[101] AM30
AD11	VSS[23]	VSS[102] AM31
AD12	VSS[24]	VSS[103] AM32
AD16	VSS[25]	VSS[104] AM33
AD23	VSS[26]	VSS[105] AM34
AD30	VSS[27]	VSS[106] AM35
AD31	VSS[28]	VSS[107] AM38
AD32	VSS[29]	VSS[108] AM39
AD34	VSS[30]	VSS[109] AM42
AU22	VSS[31]	VSS[110] AU20
AD42	VSS[32]	VSS[111] AM46
AD46	VSS[33]	VSS[112] AV22
AD49	VSS[34]	VSS[113] AM49
AD7	VSS[35]	VSS[114] AM7
AE2	VSS[36]	VSS[115] AA50
AE4	VSS[37]	VSS[116] BB10
AE12	VSS[38]	VSS[117] AN32
Y13	VSS[39]	VSS[118] AN50
AH49	VSS[40]	VSS[119] AN62
AL4	VSS[41]	VSS[120] AP12
AF35	VSS[42]	VSS[121] AP42
AP13	VSS[43]	VSS[122] AP46
AN34	VSS[44]	VSS[123] AP49
AE45	VSS[45]	VSS[124] AP5
AF46	VSS[46]	VSS[125] AR2
AF49	VSS[47]	VSS[126] AR52
AF5	VSS[48]	VSS[127] AT11
AF8	VSS[49]	VSS[128] BA12
AG2	VSS[50]	VSS[129] AH48
AG52	VSS[51]	VSS[130] AT32
AH11	VSS[52]	VSS[131] AT36
AH15	VSS[53]	VSS[132] AT41
AH16	VSS[54]	VSS[133] AT47
AH24	VSS[55]	VSS[134] AT7
AH32	VSS[56]	VSS[135] AV12
AV18	VSS[57]	VSS[136] AV16
AH43	VSS[58]	VSS[137] AV20
AH47	VSS[59]	VSS[138] AV24
AH7	VSS[60]	VSS[139] AV30
AJ19	VSS[61]	VSS[140] AV34
AJ2	VSS[62]	VSS[141] AV38
AJ20	VSS[63]	VSS[142] AV42
AJ22	VSS[64]	VSS[143] AV46
AJ26	VSS[65]	VSS[144] AV5
AJ32	VSS[66]	VSS[145] AV8
AJ34	VSS[67]	VSS[146] AW14
AT5	VSS[68]	VSS[147] AW18
AJ4	VSS[69]	VSS[148] AW2
AK12	VSS[70]	VSS[149] AW32
AM41	VSS[71]	VSS[150] AW36
AN19	VSS[72]	VSS[151] AW40
AK26	VSS[73]	VSS[152] AW52
AK22	VSS[74]	VSS[153] AY11
AK23	VSS[75]	VSS[154] AY43
AK28	VSS[76]	VSS[155] AY47
AK28	VSS[77]	VSS[156]
AK28	VSS[78]	VSS[157]
AK28	VSS[79]	VSS[158]

IbexPeak-M\_R1P0

U40I

AY7	VSS[159]	VSS[259] H49
B11	VSS[160]	VSS[260] H5
B15	VSS[161]	VSS[261] J24
B19	VSS[162]	VSS[262] K11
B23	VSS[163]	VSS[263] K43
B31	VSS[164]	VSS[264] K47
B35	VSS[165]	VSS[265] L14
B39	VSS[166]	VSS[266] L18
B43	VSS[167]	VSS[267] L2
B47	VSS[168]	VSS[268] L22
B7	VSS[169]	VSS[269] L32
BG12	VSS[170]	VSS[270] L36
BB12	VSS[171]	VSS[271] L40
BB16	VSS[172]	VSS[272] L52
BB20	VSS[173]	VSS[273] M12
BB24	VSS[174]	VSS[274] M16
BB30	VSS[175]	VSS[275] M20
BB34	VSS[176]	VSS[276] M34
BB38	VSS[177]	VSS[277] M38
BB42	VSS[178]	VSS[278] M42
BB49	VSS[179]	VSS[279] M46
BB5	VSS[180]	VSS[280] M49
BC10	VSS[181]	VSS[281] M5
BC14	VSS[182]	VSS[282] M8
BC18	VSS[183]	VSS[283] N24
BC2	VSS[184]	VSS[284] P11
BC22	VSS[185]	VSS[285] AD15
BC32	VSS[186]	VSS[286] P22
BC36	VSS[187]	VSS[287] P30
BC40	VSS[188]	VSS[288] P32
BC44	VSS[189]	VSS[289] P34
BC52	VSS[190]	VSS[290] P42
BH9	VSS[191]	VSS[291] P46
BD48	VSS[192]	VSS[292] P47
BD49	VSS[193]	VSS[293] R2
BD5	VSS[194]	VSS[294] R52
BE12	VSS[195]	VSS[295] T12
BE16	VSS[196]	VSS[296] T41
BE20	VSS[197]	VSS[297] T46
BE24	VSS[198]	VSS[298] T49
BE30	VSS[199]	VSS[299] T5
BE34	VSS[200]	VSS[300] T8
BE38	VSS[201]	VSS[301] U30
BE42	VSS[202]	VSS[302] U32
BE46	VSS[203]	VSS[303] U34
BE50	VSS[204]	VSS[304] V11
BE6	VSS[205]	VSS[305] V16
BE6	VSS[206]	VSS[306] V19
BE8	VSS[207]	VSS[307] V20
BF3	VSS[208]	VSS[308] V22
BF51	VSS[209]	VSS[309] V30
BG18	VSS[210]	VSS[310] V31
RG24	VSS[211]	VSS[311] V32
RG4	VSS[212]	VSS[312] V34
RG50	VSS[213]	VSS[313] V35
BH11	VSS[214]	VSS[314] V38
BH15	VSS[215]	VSS[315] V43
BH19	VSS[216]	VSS[316] V45
BH23	VSS[217]	VSS[317] V46
BH31	VSS[218]	VSS[318] V47
BH35	VSS[219]	VSS[319] V49
BH39	VSS[220]	VSS[320] V5
BH43	VSS[221]	VSS[321] V7
BH47	VSS[222]	VSS[322] V8
BA12	VSS[223]	VSS[323] W2
C12	VSS[224]	VSS[324] W52
C50	VSS[225]	VSS[325] Y11
D51	VSS[226]	VSS[326] Y12
E12	VSS[227]	VSS[327] Y15
E16	VSS[228]	VSS[328] Y19
E20	VSS[229]	VSS[329] Y23
E24	VSS[230]	VSS[330] Y28
E30	VSS[231]	VSS[331] Y30
E32	VSS[232]	VSS[332] Y31
E34	VSS[233]	VSS[333] Y32
E38	VSS[234]	VSS[334] Y33
E42	VSS[235]	VSS[335] Y34
E46	VSS[236]	VSS[336] Y35
E48	VSS[237]	VSS[337] Y38
E6	VSS[238]	VSS[338] Y43
F49	VSS[239]	VSS[339] Y46
F5	VSS[240]	VSS[340] P49
G10	VSS[241]	VSS[341] Y5
G12	VSS[242]	VSS[342] Y6
G14	VSS[243]	VSS[343] Y8
G18	VSS[244]	VSS[344] P24
G2	VSS[245]	VSS[345] T43
G22	VSS[246]	VSS[346] AD51
G32	VSS[247]	VSS[347] ATR
G36	VSS[248]	VSS[348] AD47
G40	VSS[249]	VSS[349] Y47
G44	VSS[250]	VSS[350] AT12
G52	VSS[251]	VSS[351] AM6
AF39	VSS[252]	VSS[352] AT13
H16	VSS[253]	VSS[353] AM5
H20	VSS[254]	VSS[354] AK45
H30	VSS[255]	VSS[355] AK38
H34	VSS[256]	VSS[356] AV14
H38	VSS[257]	
H42	VSS[258]	

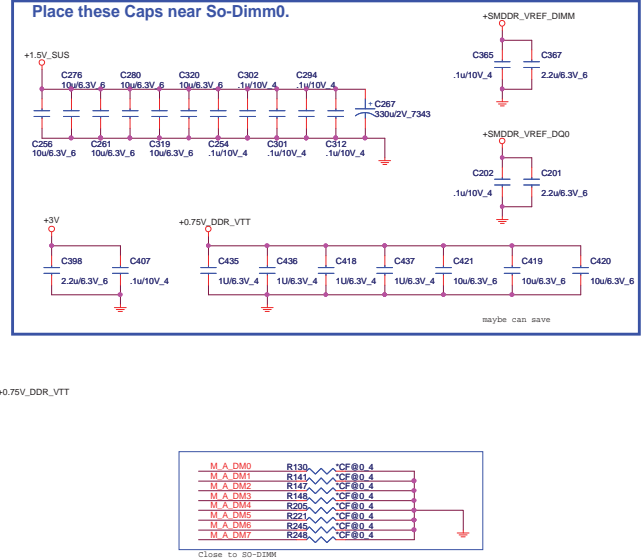
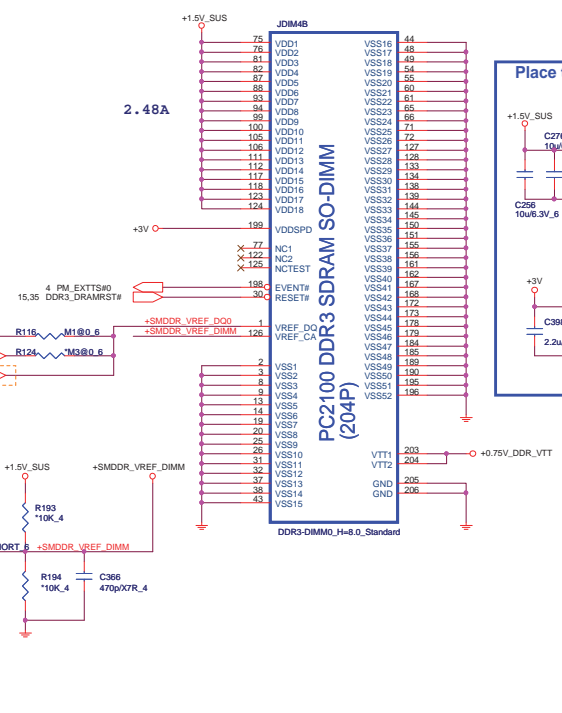
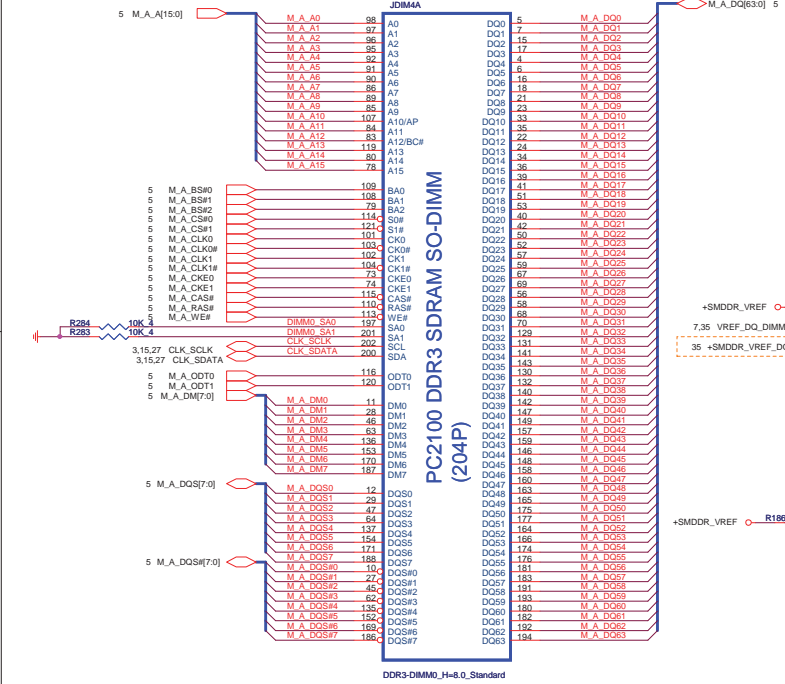
IbexPeak-M\_R1P0



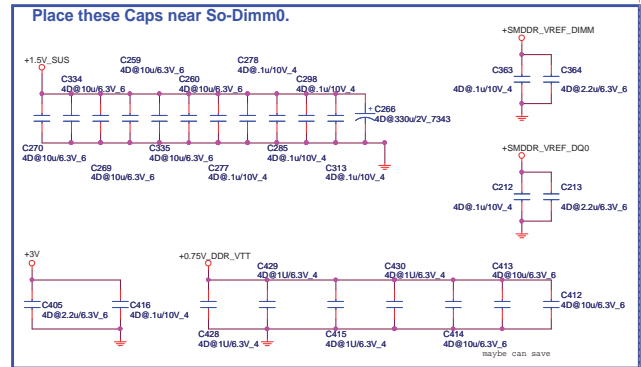
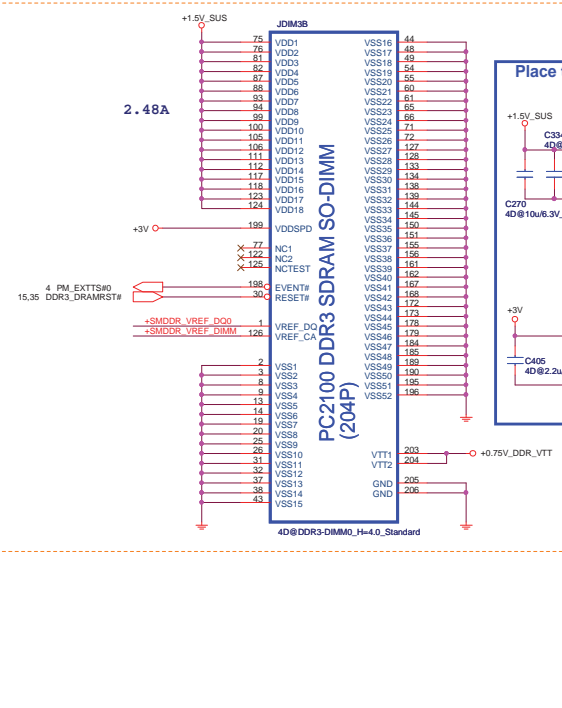
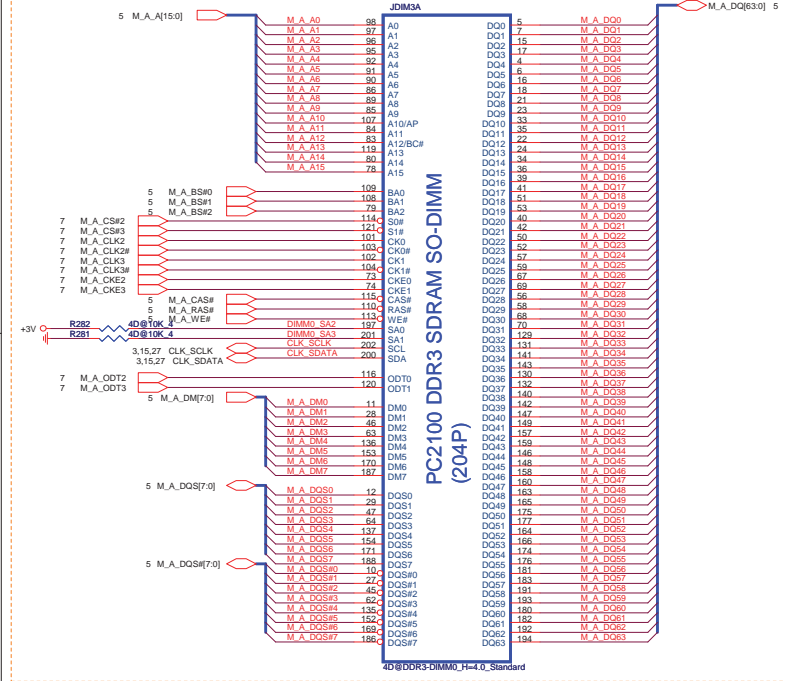
**Quanta Computer Inc.**  
PROJECT : ZR7

Size	Document Number	Rev
	<b>IBEX PEAK-M 6/6</b>	<b>3B</b>
Date:	Monday, February 22, 2010	Sheet 13 of 49



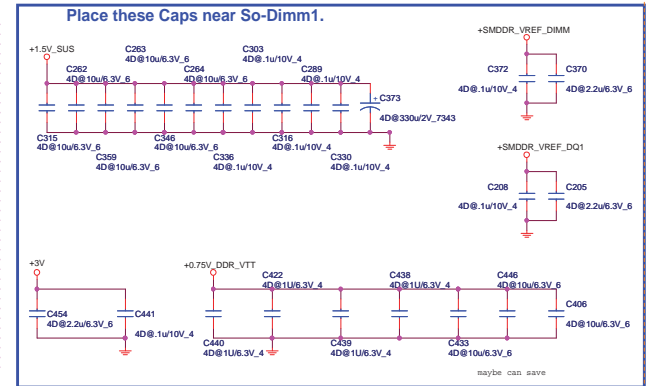
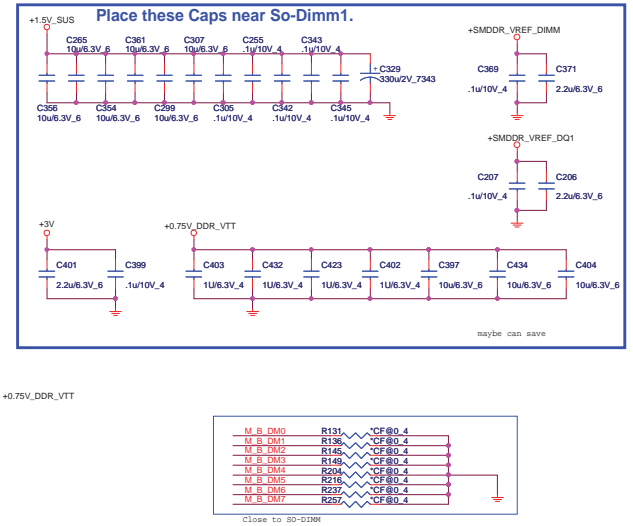
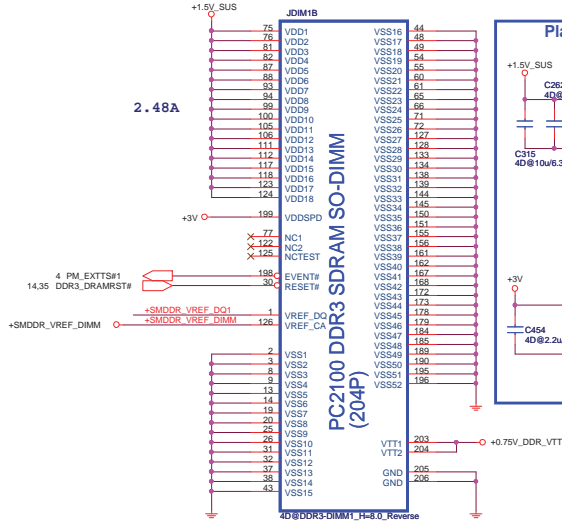
**DIMM A0**

**DIMM A1** 4D@ --> 4 SO-DIMM





**DIMM B1** 4D@ --> 4 SO-DIMM



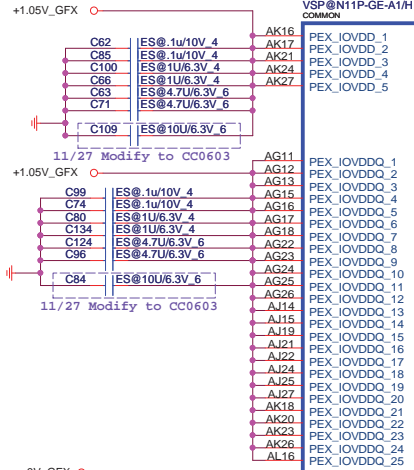
PEX\_IOVDD+PEX\_IOVDDQ+PEX\_PLLVDD >2.2A

~ 500mA

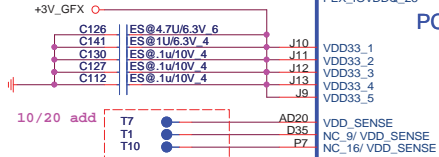
1600mA

Near BGA

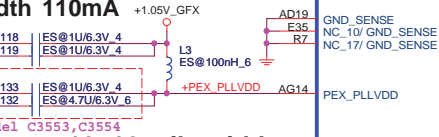
U33A  
VSP@N11P-GE-A1/H  
COMMON



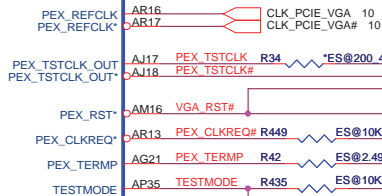
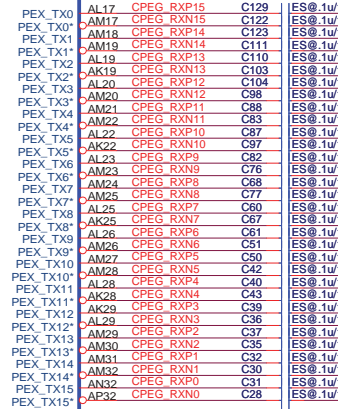
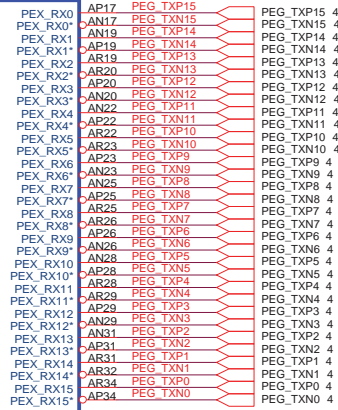
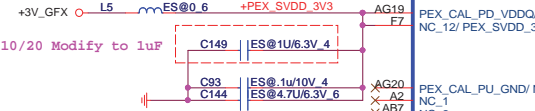
PCI EXPRESS



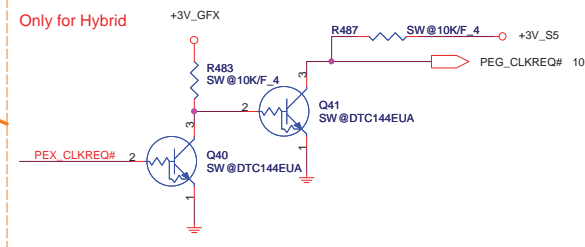
12~16 mils width 110mA



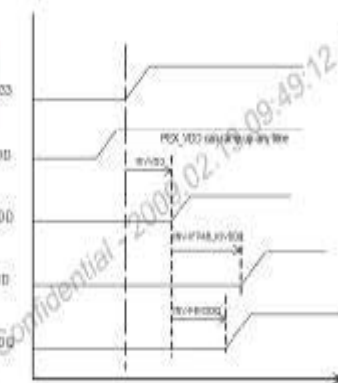
12~16 mils width



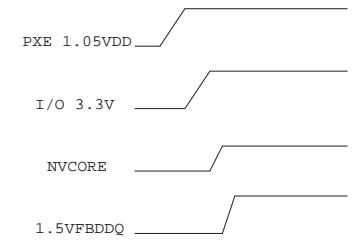
SW@ --> iGPU & dGPU Switch



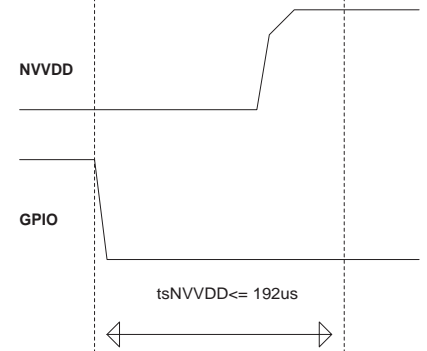
EV@ --> dGPU only  
SW@ --> iGPU & dGPU Switch  
ES@ --> External VGA SKU  
VSP@ --> Operation P/N (VGA)



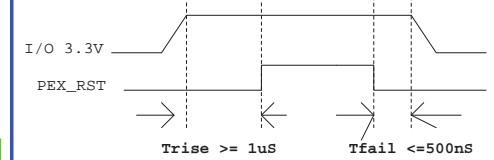
power up sequence



NB9M: VGACORE +0.90V (Normal), +1.09V  
NVVDD Maximum Settling Time




PEX\_RST timing





VSP@ --> Operation P/N (VGA) 11EP@ --> N11P/N11E-GE1 Setting  
ES@ --> External VGA SKU U33B 12/


U33B


12/02 modify  
package for N10


21 VMA\_DQ[63..0] 


21 VMA\_DM[7..0] 


21 VMA\_WDQS[7..0] 

21 VMA\_RDQS[7..0] 

22 VMC\_DQ[63..0] 

22 VMC\_DM[7..0] 

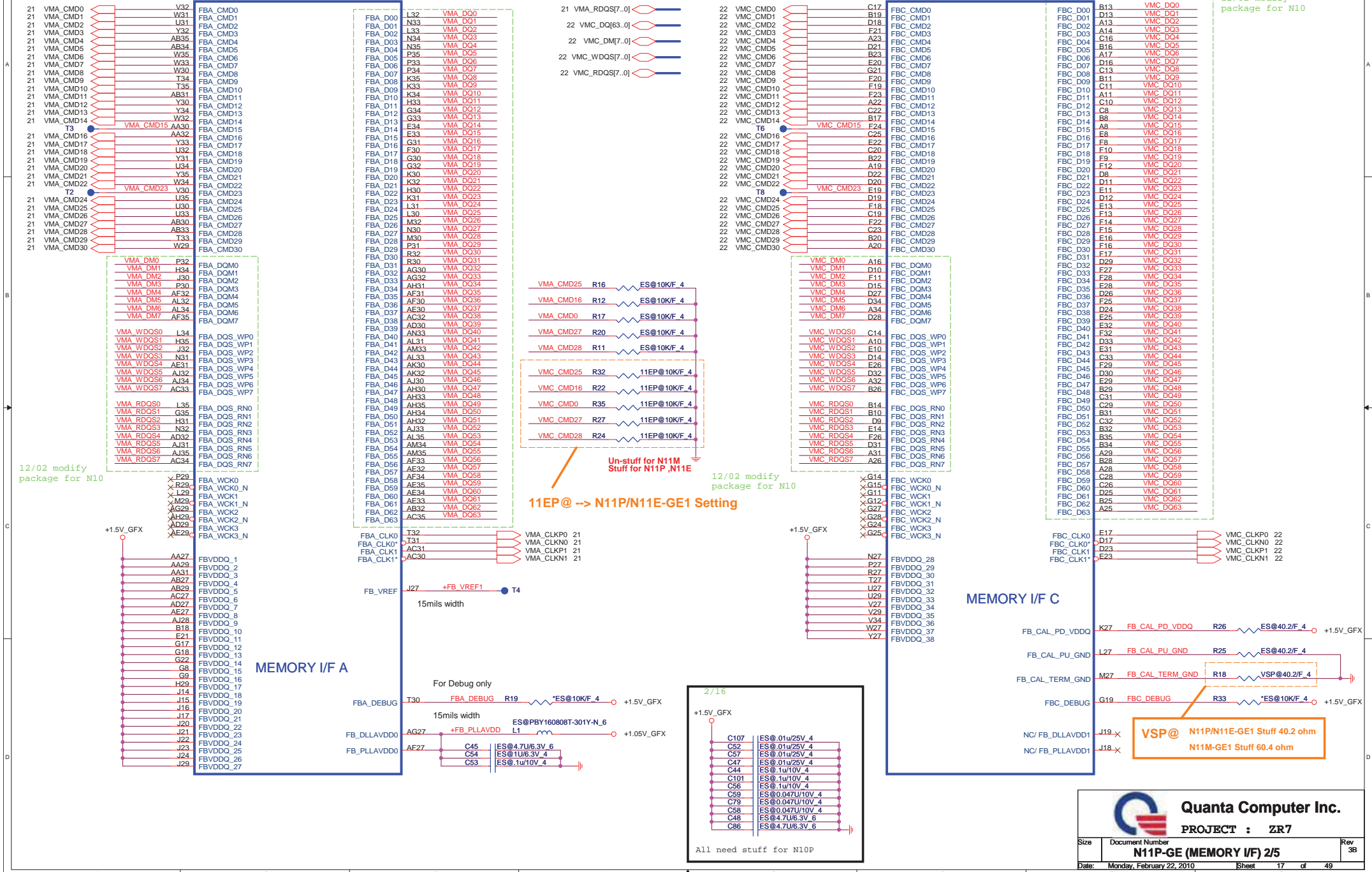
22 VMC\_WDQS[7..0] 

22 VMC\_RDQS[7..0] 

U33

973-nvidia-n11p-es-a  
MON

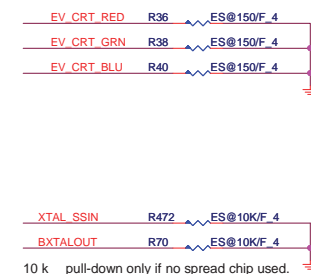
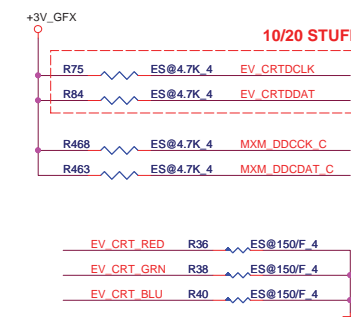
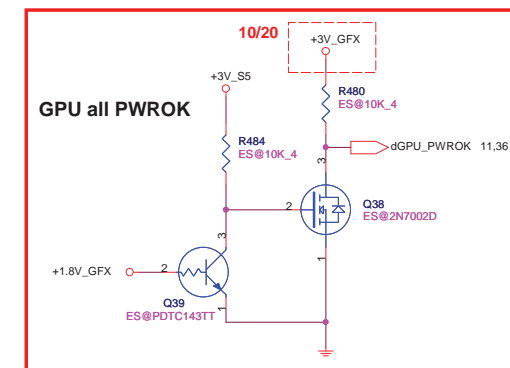
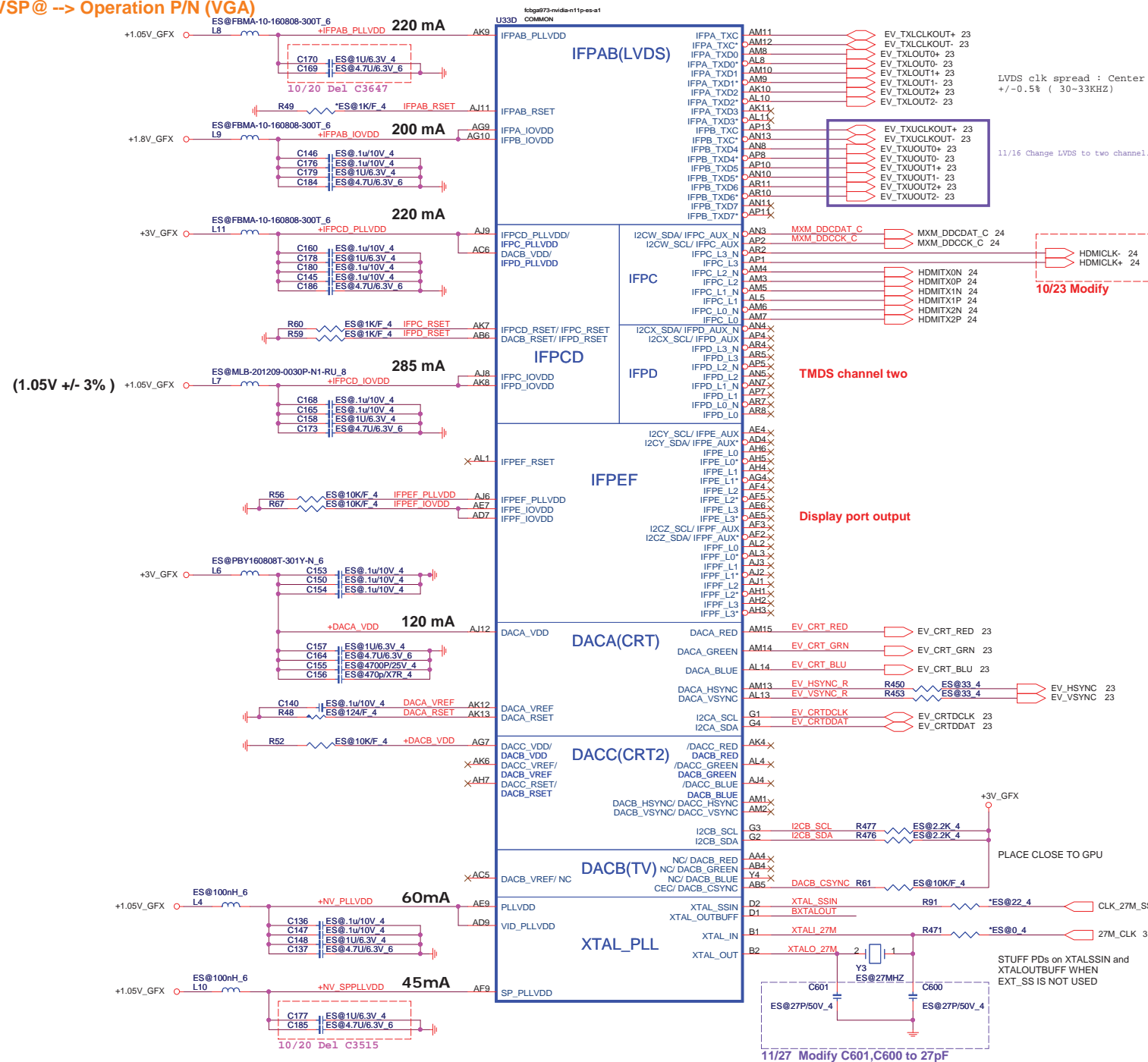
```
12/02 modify
package for N10
```

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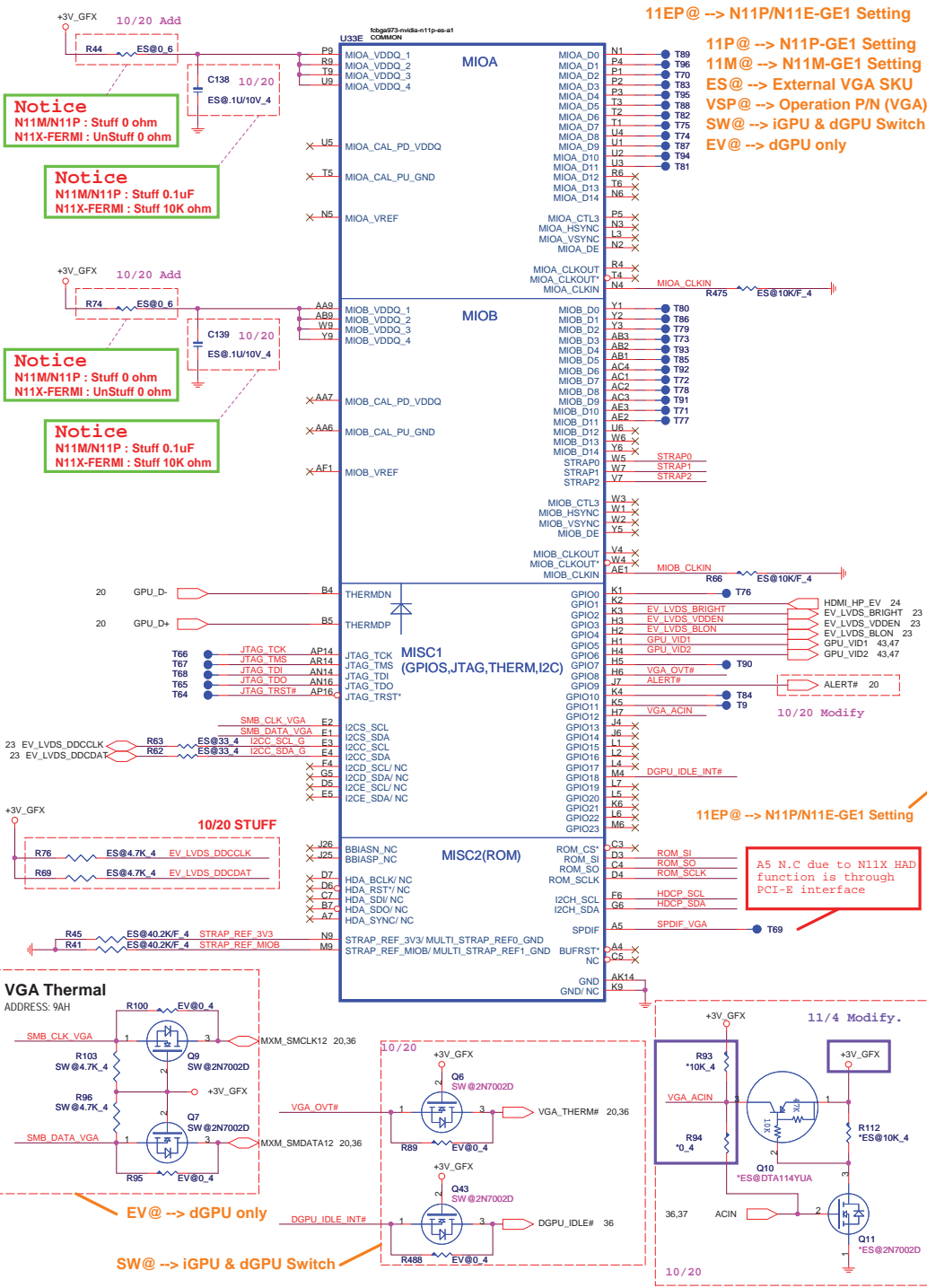
PROJECT : ZR7

Size	Document Number <b>N11P-GE (MEMORY I/F) 2/5</b>	Rev 3E
Date	Monday, February 22, 2010	Sheet 17 of 49

ES@ --> External VGA SKU  
VSP@ --> Operation P/N (VGA)

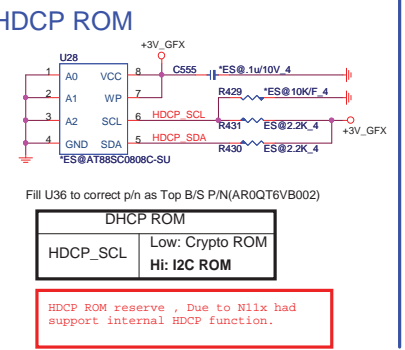
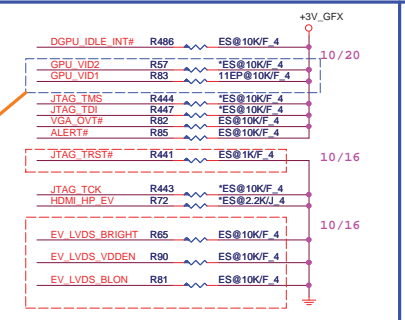
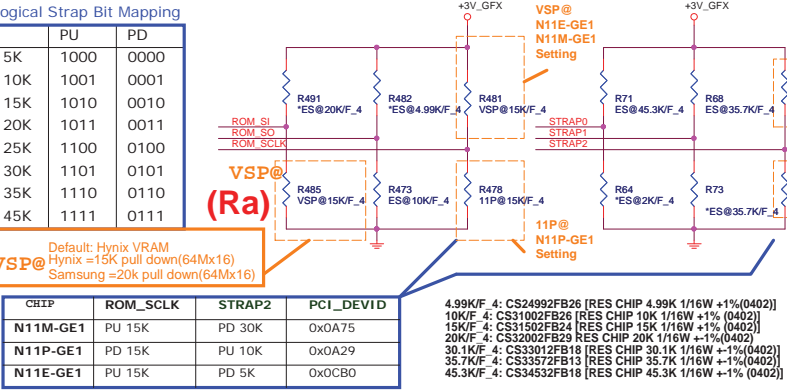






	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	X010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	1110
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI	(Ra)
0000	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Reserved	IDGH1G-04A1F1C-16X	PD 10K	AKDSLZGTW04
0001	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix	H5K1G63BFR-12C	PD 15K	AKDSLZGTW04
0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung	K4W1G1646E-HC12	PD 20K	AKDSLZGTW04
0100		Reserved			
0101		Reserved			
0110		Reserved			
XXXX					
XXXX					

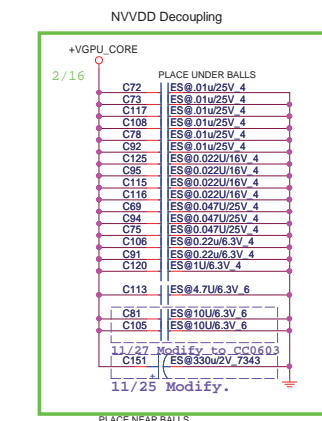
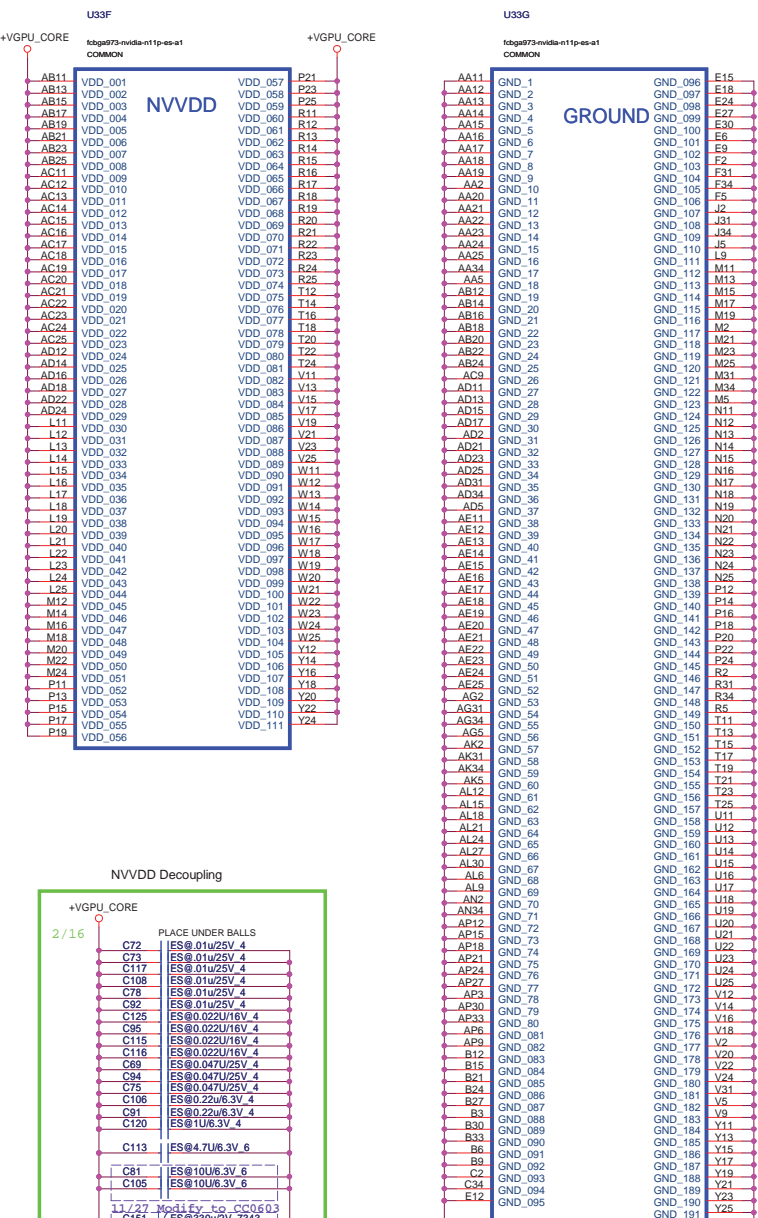
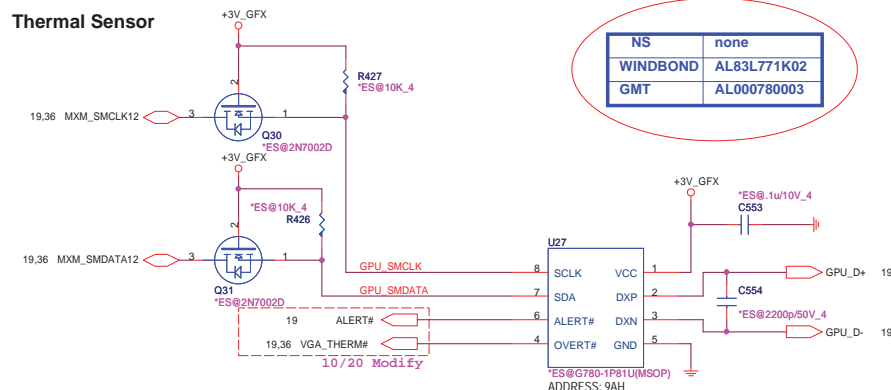


GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	Hot plug detect for IFP link C
1	IN	N/A	PANEL BACKLIGHT PWM
2	OUT	HIGH	PANEL POWER ENABLE
3	OUT	HIGH	PANEL BACKLIGHT ENABLE
4	OUT	N/A	NVDD VID0
5	OUT	N/A	NVDD VID1
6	OUT	N/A	NVDD VID2 11/13
7	I/O	LOW	OVERT
8	I/O	LOW	ALERT
9	OUT	N/A	FBVREF SELECT
10	OUT	N/A	SLI SYNC0
11	IN	N/A	PWR_LEVEL 11/13
12	OUT	N/A	MEM_VID or power supply control
13	OUT	N/A	PS CONTROL
14	OUT	N/A	

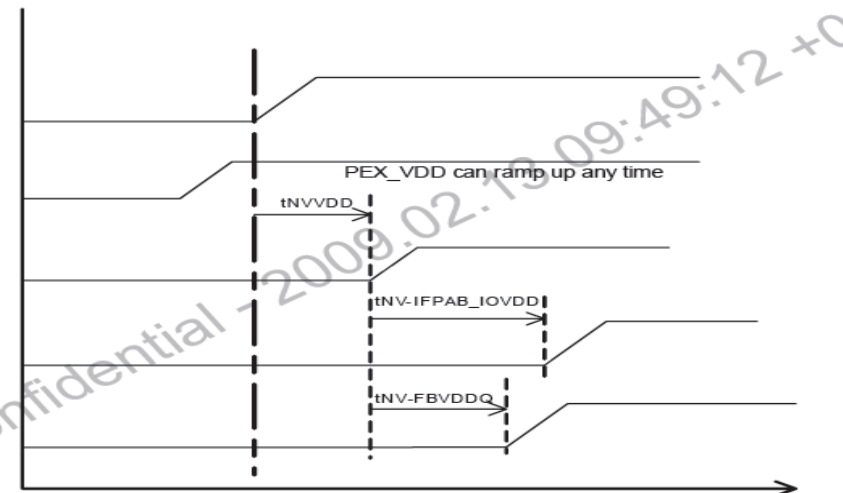
ES@ --> External VGA SKU  
VSP@ --> Operation P/N (VGA)

# Thermal Sensor

NS	none
WINDBOND	AL83L771K02
GMT	AL000780003



**+3V** VDD33  
**+1.05V** PEX\_VDD  
**V\_CORE** NVVDD  
**+1.8V** IFPAB\_IOVDD  
**+1.5V** FBVDDQ



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PROJECT : ZR7

Size	Document Number	Rev
	N11P-GE (POWER & GND&THM) 5/5	38

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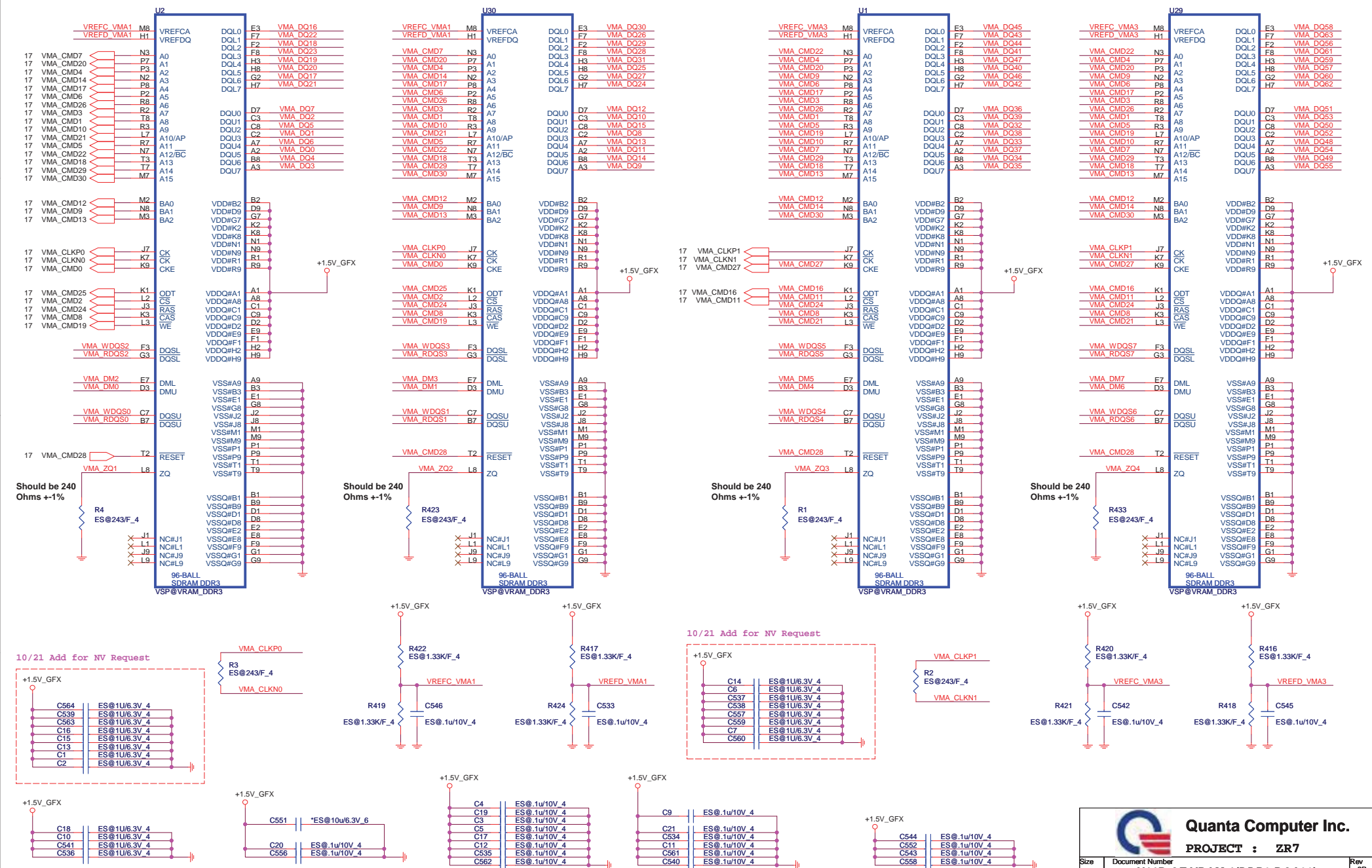
**VSP@ --> Operation P/N (VGA-VRAM)**

```

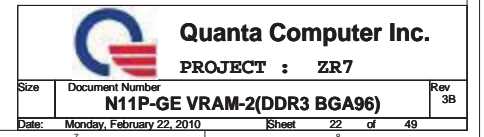
17 VMA_DQ[63..0]
17 VMA_DM[7..0]
17 VMA_WDQS[7..0]
17 VMA_RDQS[7..0]

```

**CHANNEL A: 256MB/512MB DDR3**

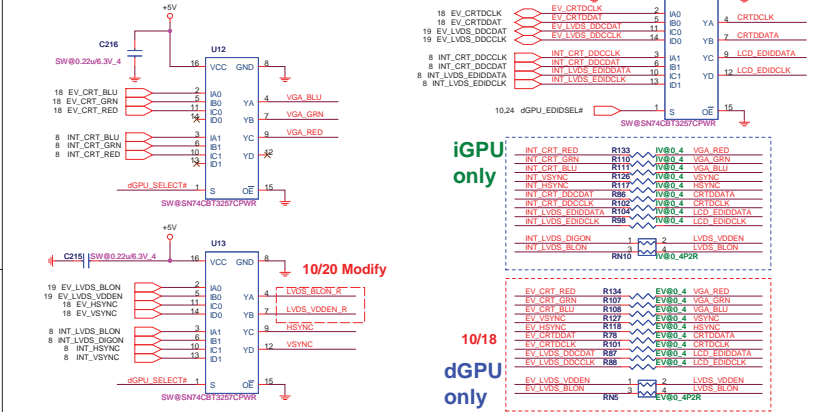


**CHANNEL B: 256MB/512MB DDR3**



- SW@ --> iGPU & dGPU Switch
- IV@ --> iGPU only
- EV@ --> dGPU only

S	Yn	dGPU_SELECT# dGPU_EDIDSEL#	Output
0	EV	L	EV_LVDS/CRT
1	IV	H	INT_LVDS/CRT

[illegible]

The diagram illustrates the hardware connections for an LCD module. Key components and their connections include:

- Capacitors:** C181 (1u10V\_4) and C190 (1000p50V\_4) are connected to the +3V supply. Another C190 (4.7u25V\_8) and C102 (1000p50V\_4) are connected to the INVC0 pin.
- Resistors:** R30 (R30) is connected to VIN. R79 (2.2K\_4) and R80 (2.2K\_4) are connected to the +3V supply and the LCD module's data pins.
- LCD Module:** The module has pins for power (VIN, GND), data (INVC0, CANS), and display control (LCD\_BRIGHT, LCD\_ENABLE, LCD\_ENABLEDATA).
- Annotations:**
  - "11/27 Add CANS pin45 to GND" indicates a modification to the wiring.
  - "1/14 Change pin3,4, define." suggests a change in the pin definitions.
  - "LCD\_BRIGHT 0.8" is a configuration parameter.

The schematic diagram illustrates the electrical connections for the LCD module. Key components include:

- Resistors:** R712 (3V), R713 (5V\_LCD), V1@0.6, V2@0.1206, C191 (1uH/3V\_4), C187 (\*SWB\_1u\_4), R99 (\*SWB100K\_4).
- Capacitors:** C196 (\*1u10V\_4), C195 (\*2.2u10V\_8), C196 (\*1u10V\_4), C197 (0.01uV\_4), C194 (22uH/3V\_8).
- Integrated Circuits:** U10 (ON/OFF), MAT4280-4.
- Other Components:** SWB0.4, J3 (\*SHORT\_PAD).

The diagram also shows power supply rails (+3V, +5V) and signal traces (EV\_LVDS\_VDDEN, INT\_LVDS\_DIGN, LB \*SWOR\_GATE). Annotations indicate modifications for different board versions: "10/22 Modify Footprint", "1/15 Add", and "10/20 Modify".

[illegible]

## iGPU HDMI LEVEL SHIFTER

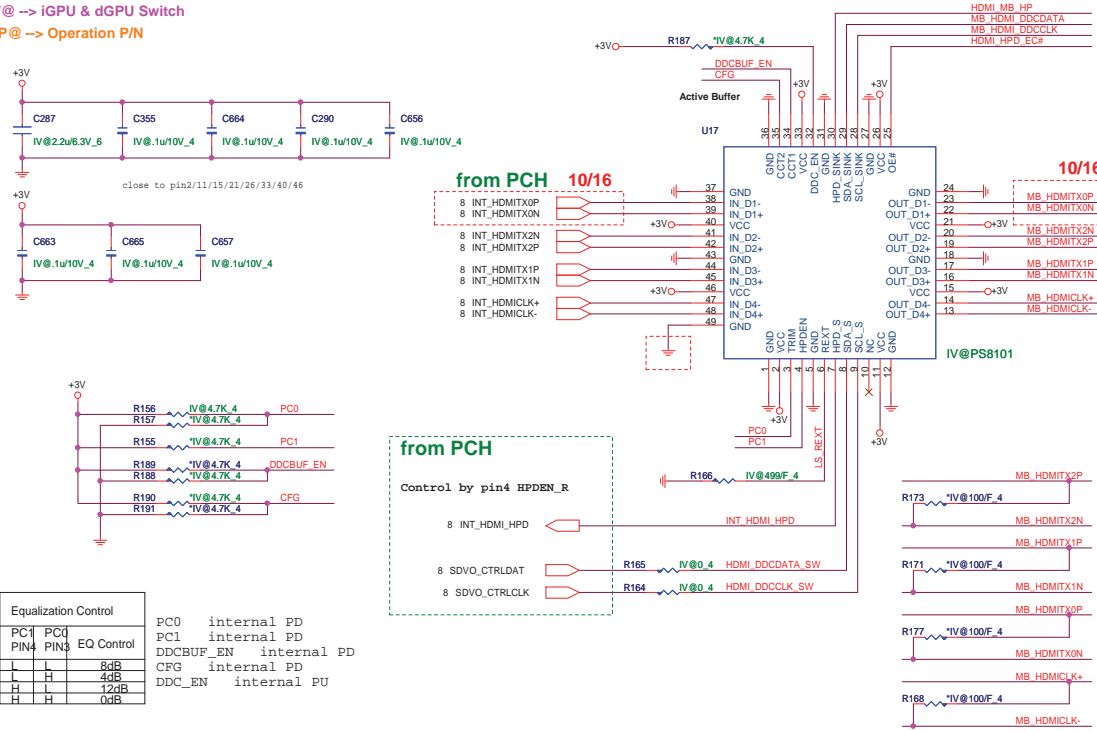
IV@ -> iGPU only

EV@ -> dGPU only

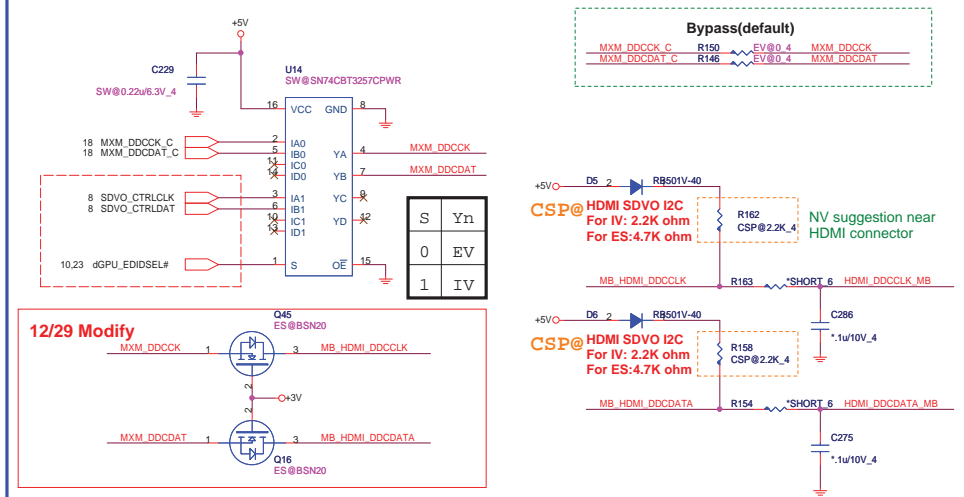
ES@ -> External VGA SKU

SW@ -> iGPU & dGPU Switch

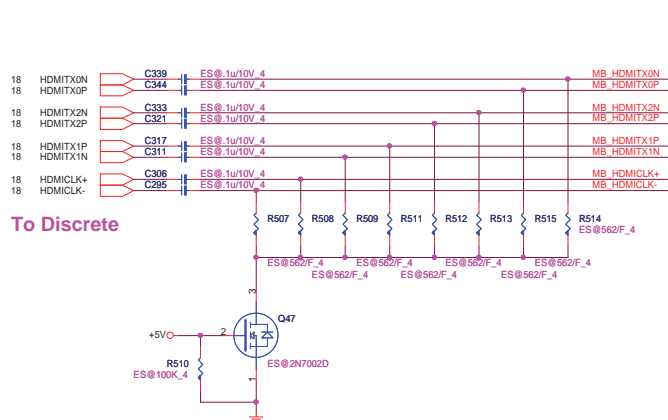
CSP@ -> Operation P/N



## SDVO I2C Control



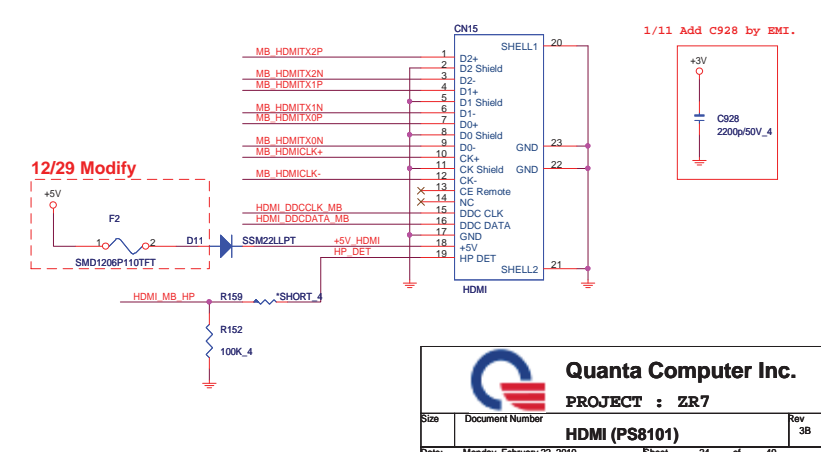
## GPU Switchable Graphic HDMI source



## ESD Protect

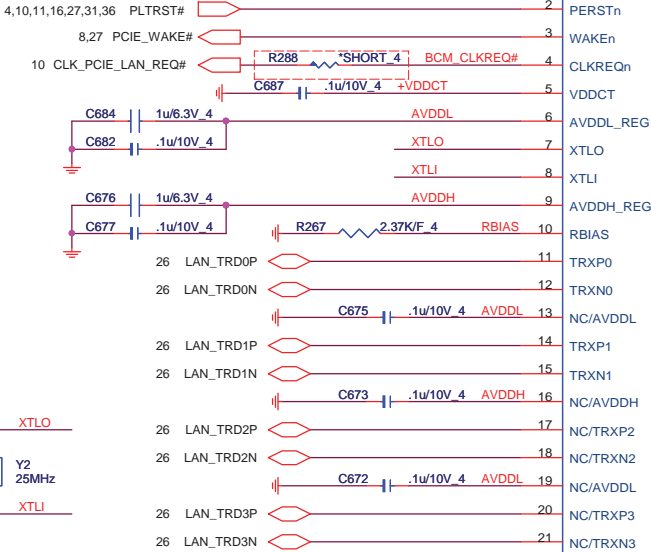
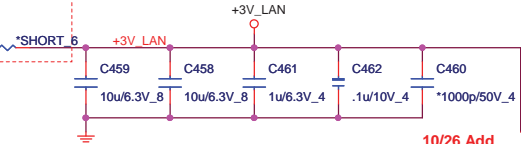
12/29 Delete U15, U16, U18.

## HDMI connector

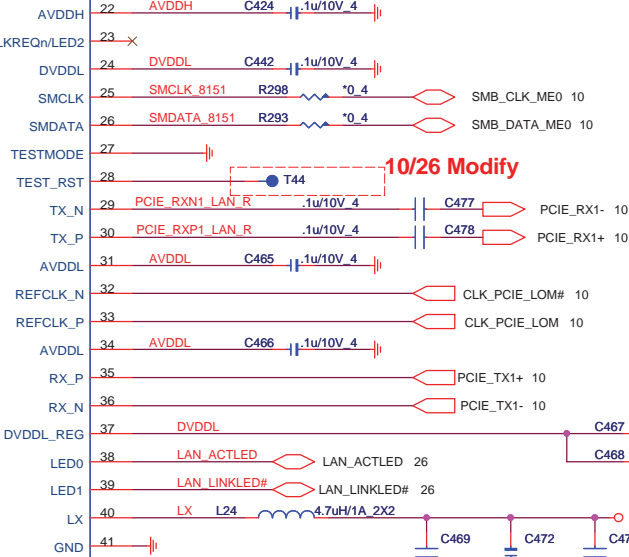


Giga-LAN AR8151

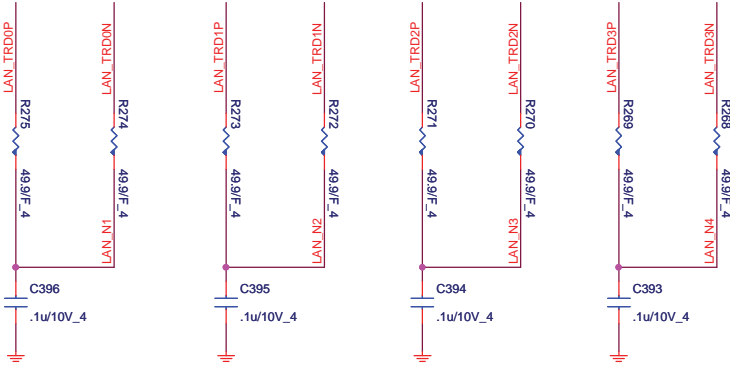
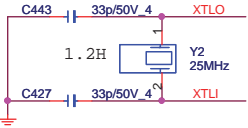
10/26 Add




AR8151  
5X5mm  
40-Pin QFN



10/26 Modify





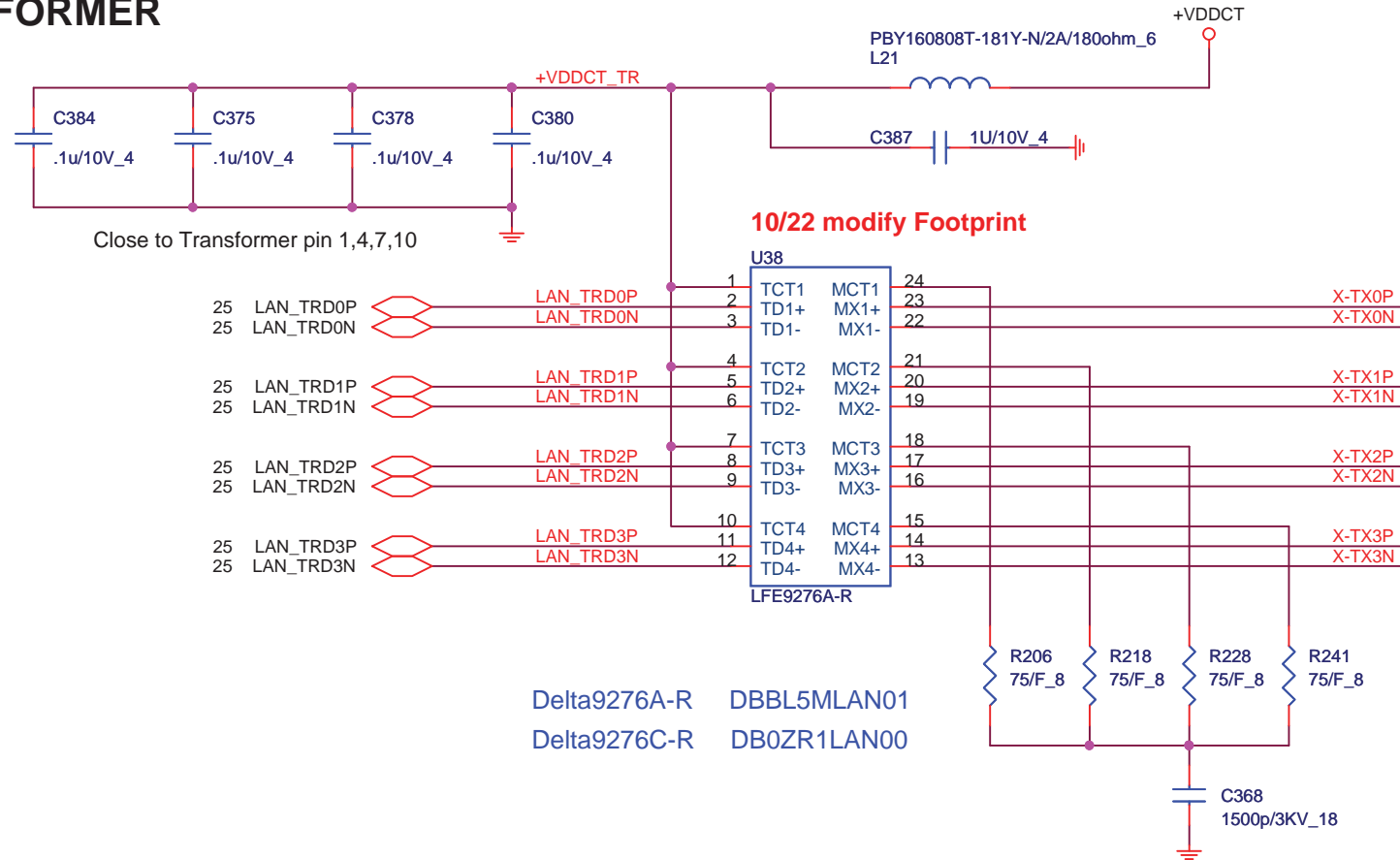
Quanta Computer Inc.

PROJECT : ZR7

GLAN BCM57780

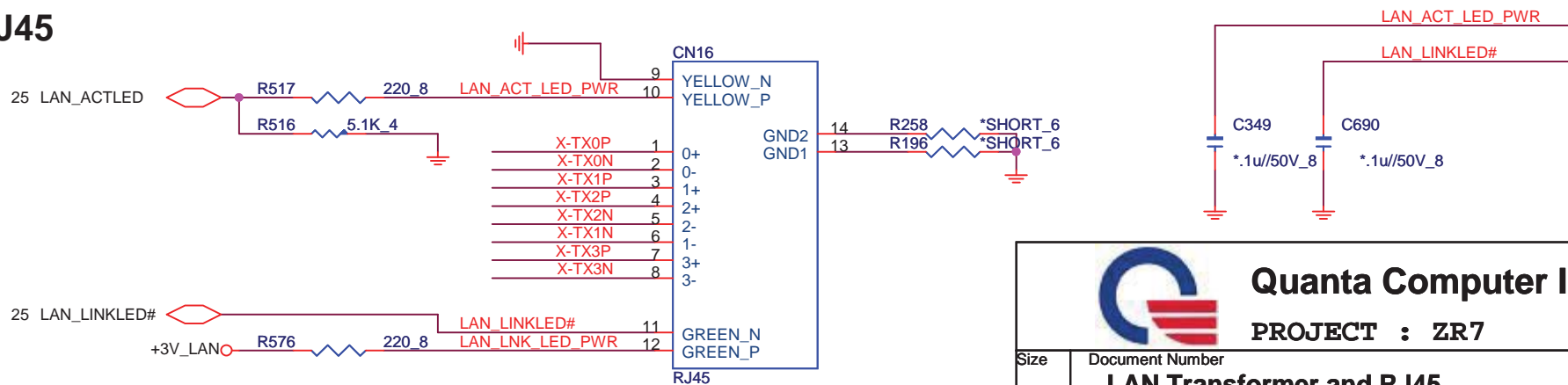
Size	Document Number	Rev
		3B
Date:	Monday, February 22, 2010	Sheet 25 of 49

# TRANSFORMER



Delta9276A-R DBBL5MLAN01  
Delta9276C-R DB0ZR1LAN00

# RJ45



**Quanta Computer Inc.**

**PROJECT : ZR7**

Size Document Number Rev  
**LAN Transformer and RJ45** 3B

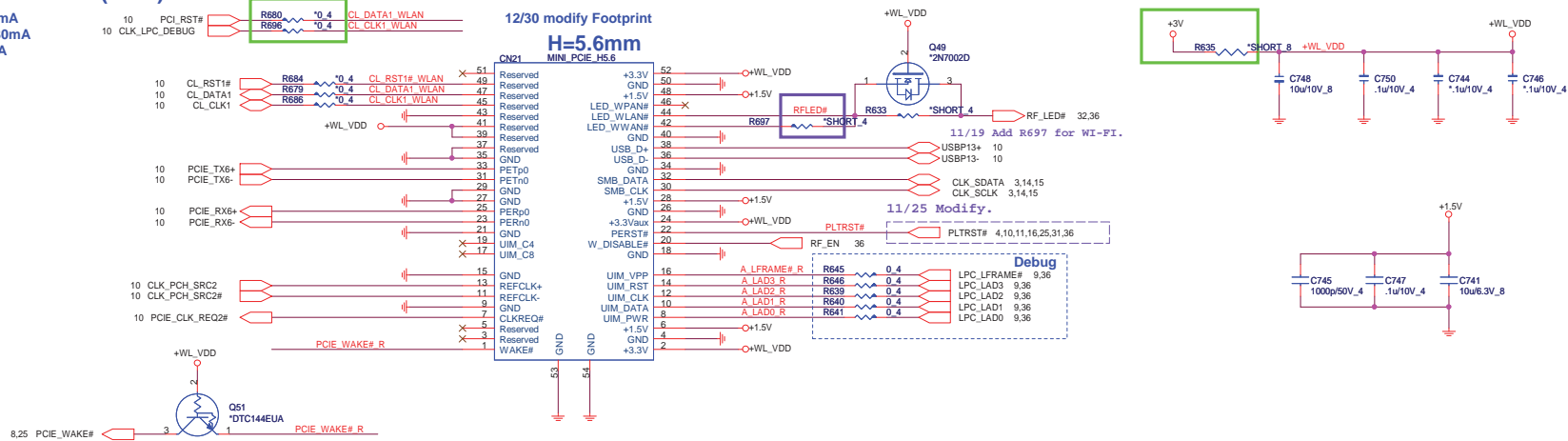
Date: Monday, February 22, 2010 Sheet 26 of 49



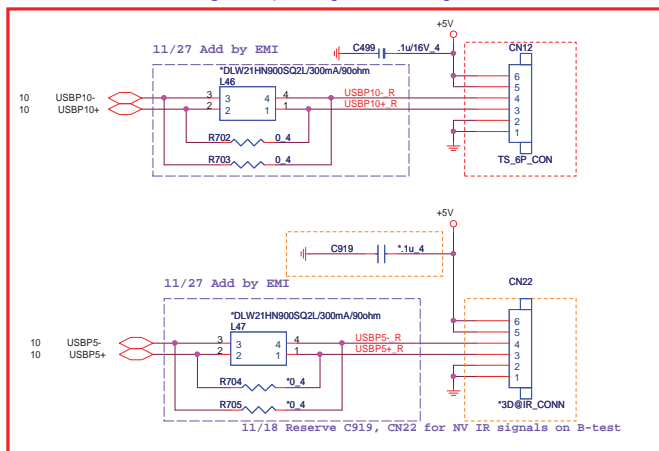
+3.3V: 1000mA  
+3.3Vaux:330mA  
+1.5V:500mA

12/30 modify Footprint

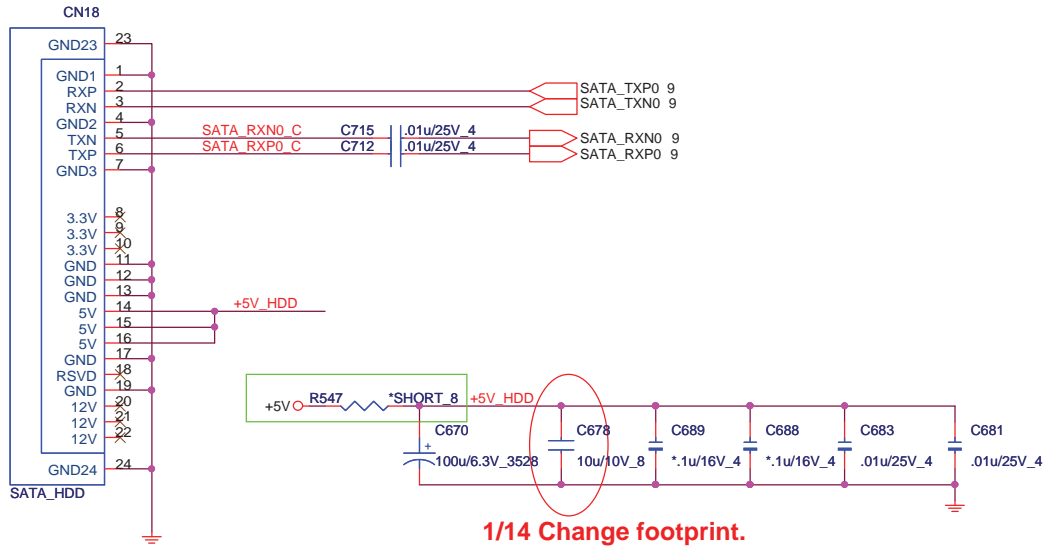
**H=5.6mm**



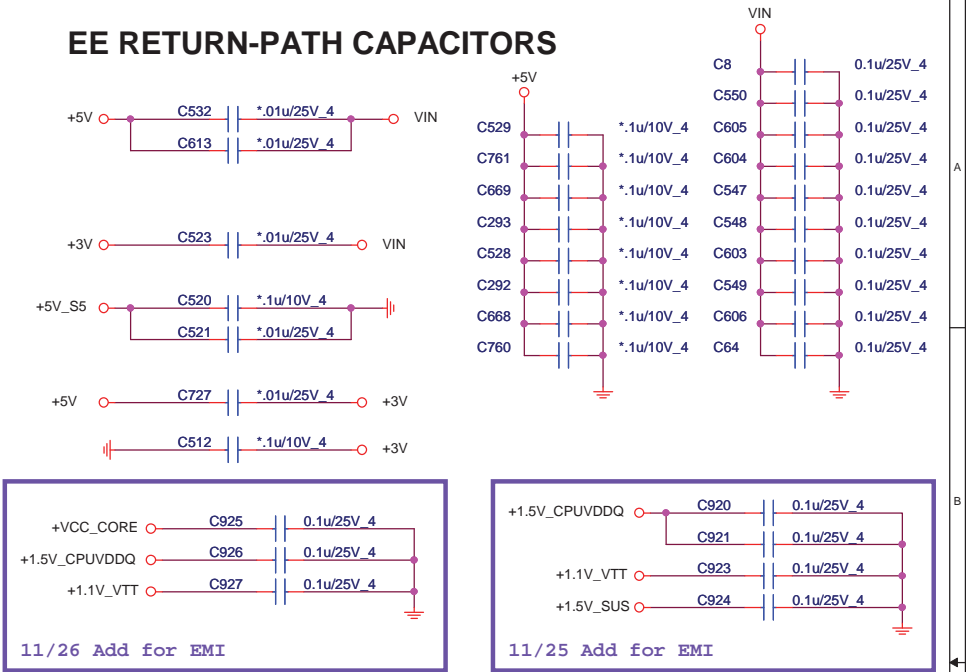
1/8 Change CN12,CN22 6pin conn footprint for Touch Screen.



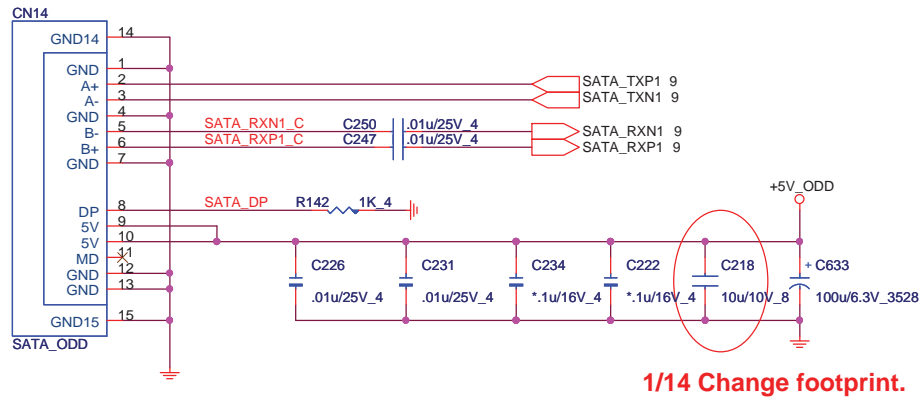
## MAIN SATA HDD



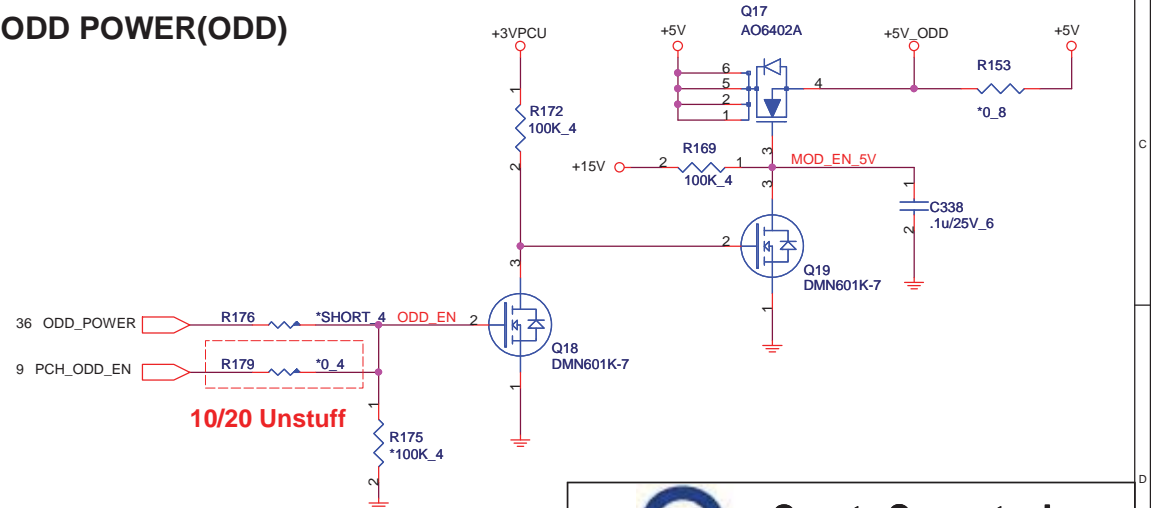
## EE RETURN-PATH CAPACITORS



## ODD (SATA)



## ODD POWER(ODD)

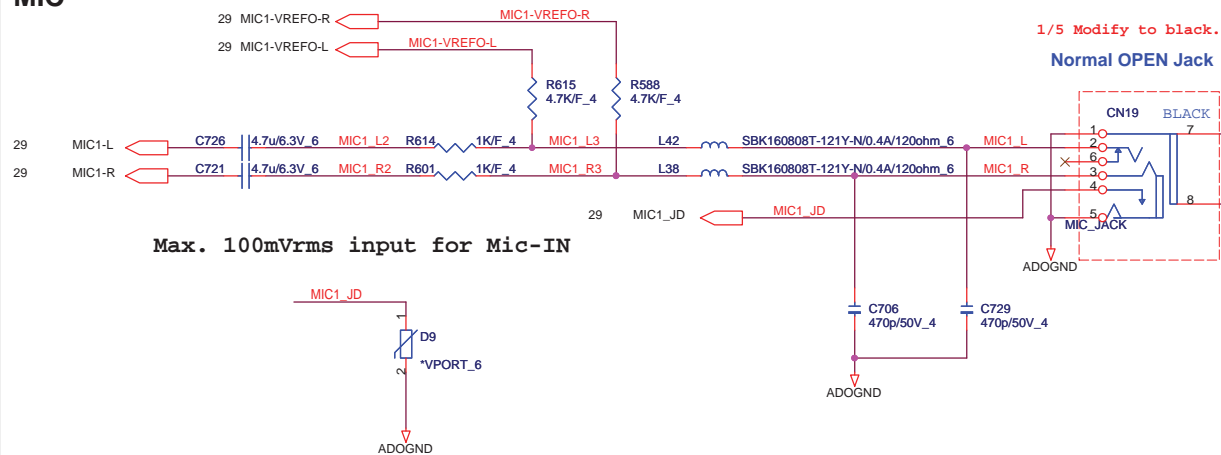


Quanta Computer Inc.

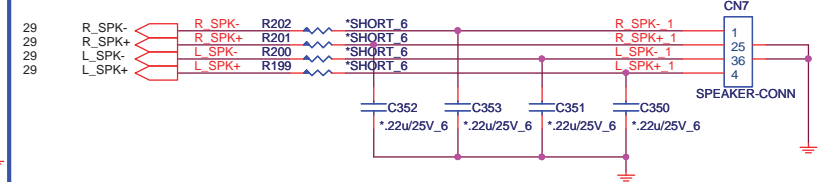
PROJECT : ZR7

Size	Document Number	Rev
	SATA-HDD/ODD/USB-ESATA	3B
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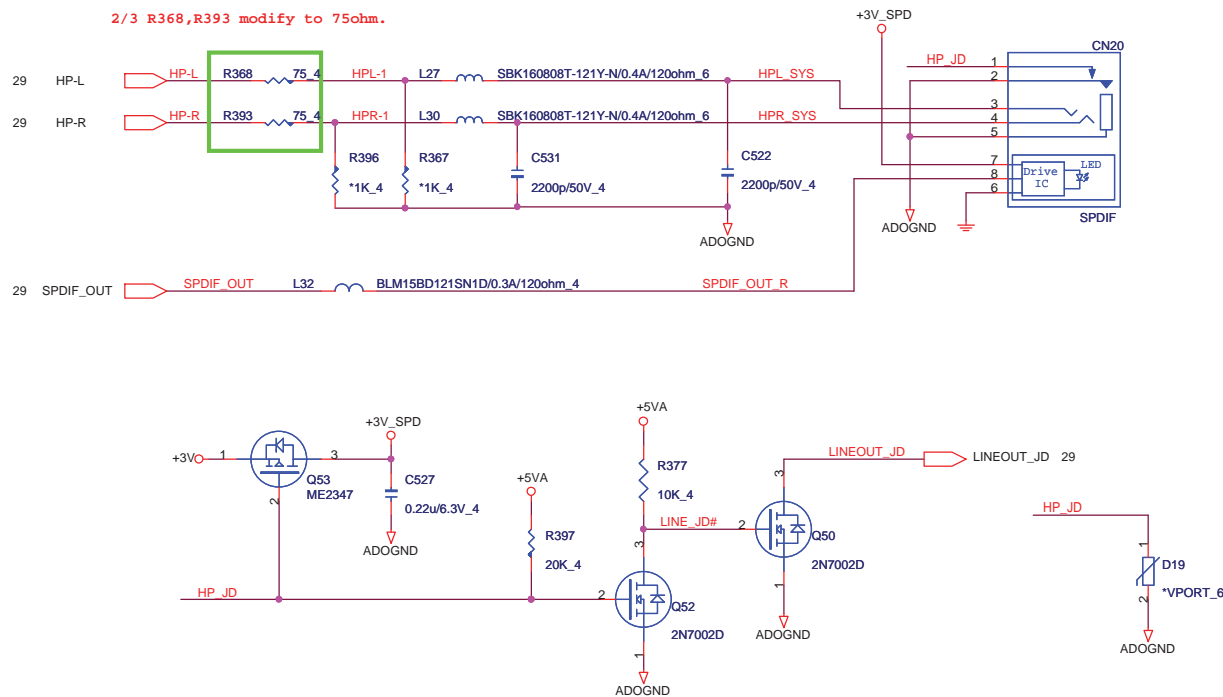



**MIC**

## Internal Speaker

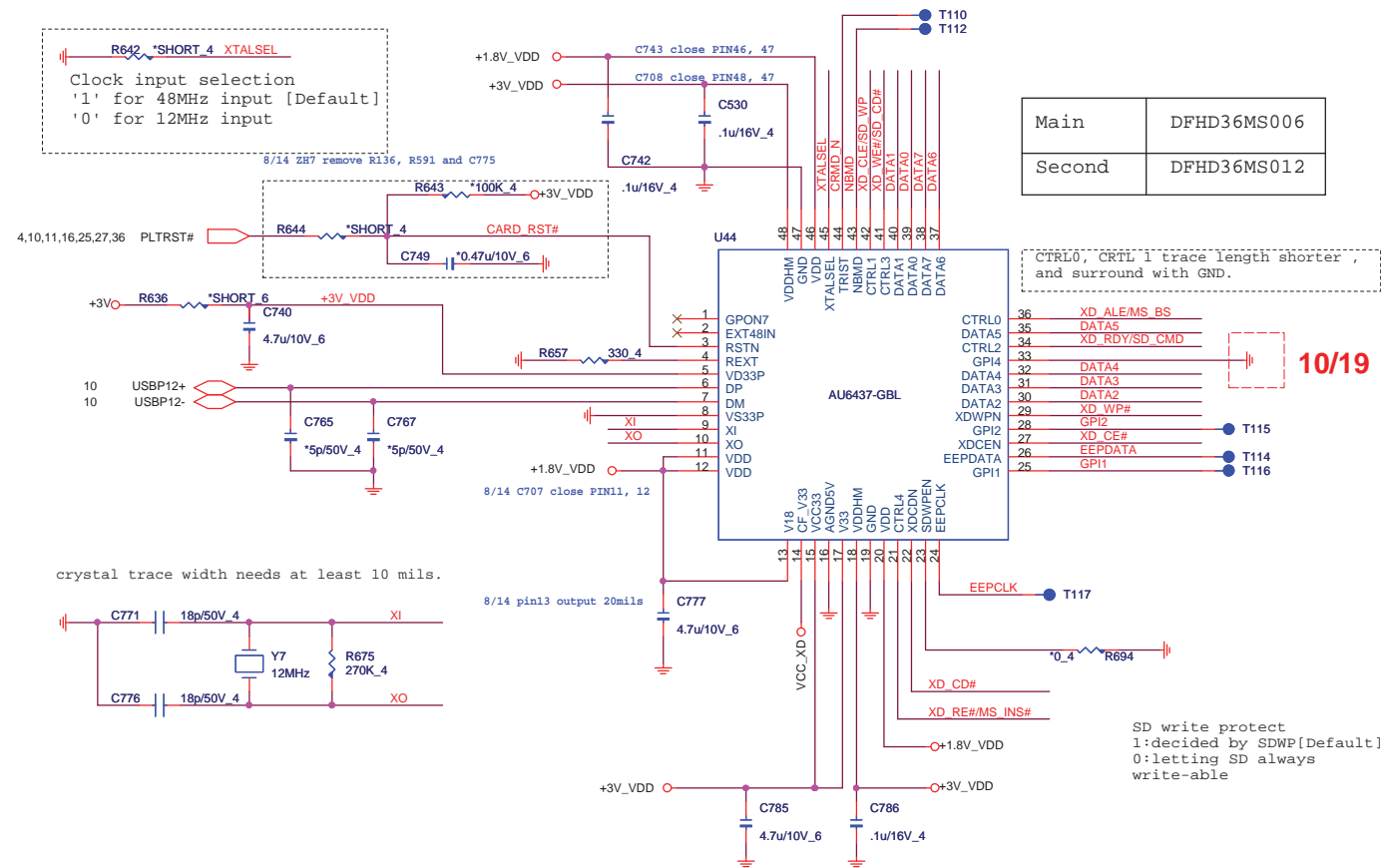


## HP/SPDIF

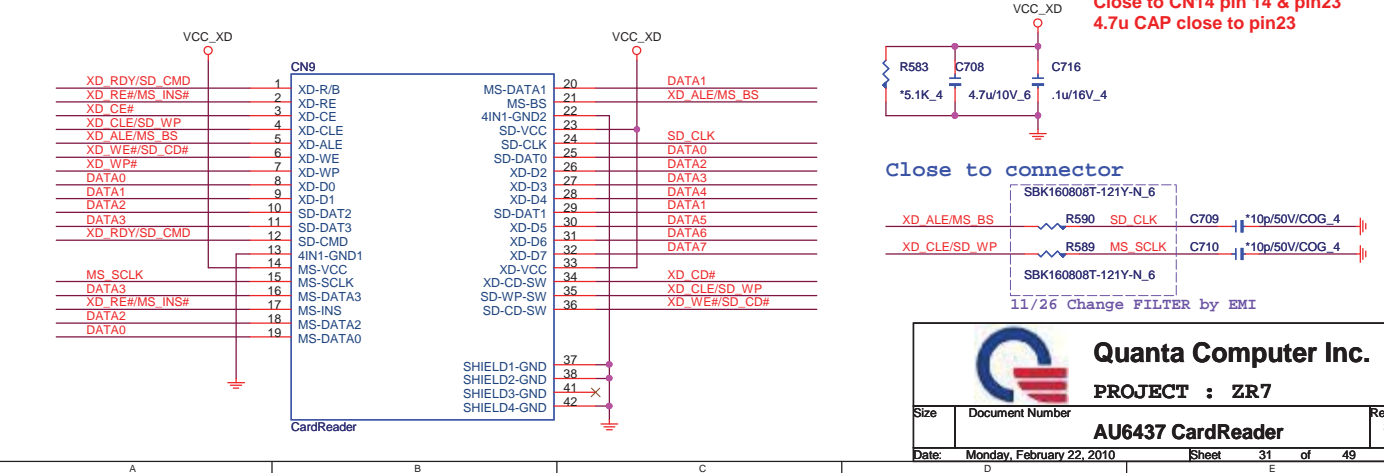


 <b>Quanta Computer Inc.</b> <b>PROJECT : ZR7</b>		
Size	Document Number	Rev 3B
<b>AMP /AUDIO JACK CONN</b>		
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# CARD READER Controller



## 4 IN 1 CARD READER (MMC)

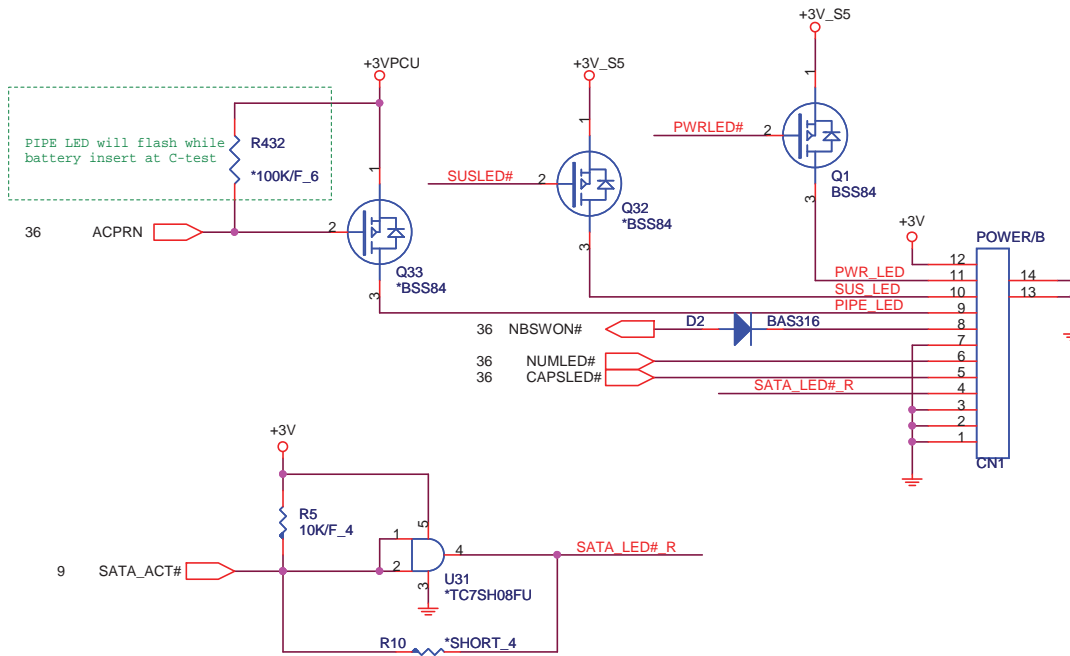


Quanta Computer Inc.

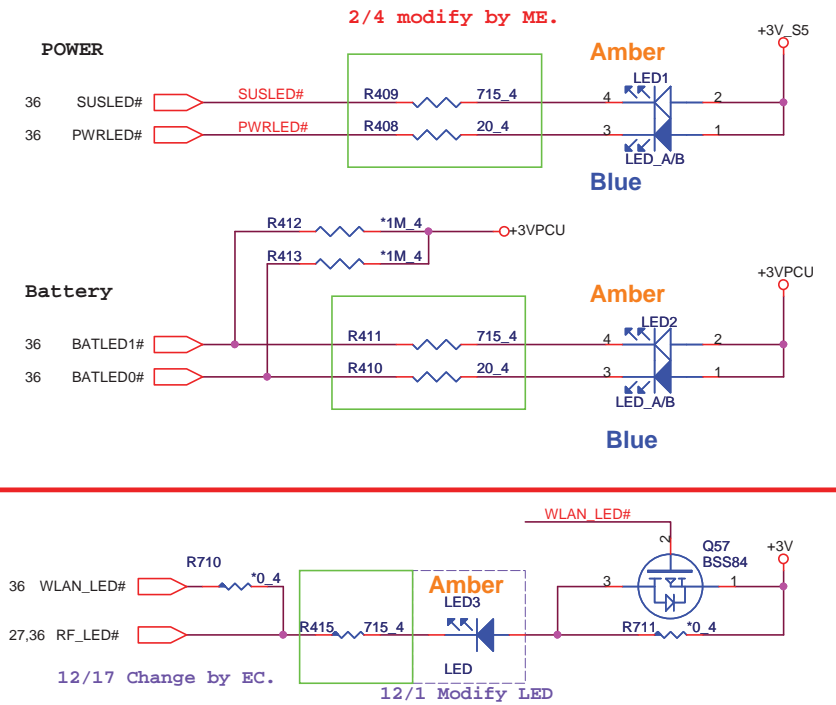
PROJECT : ZR7

Size	Document Number	Rev
	AU6437 CardReader	3B
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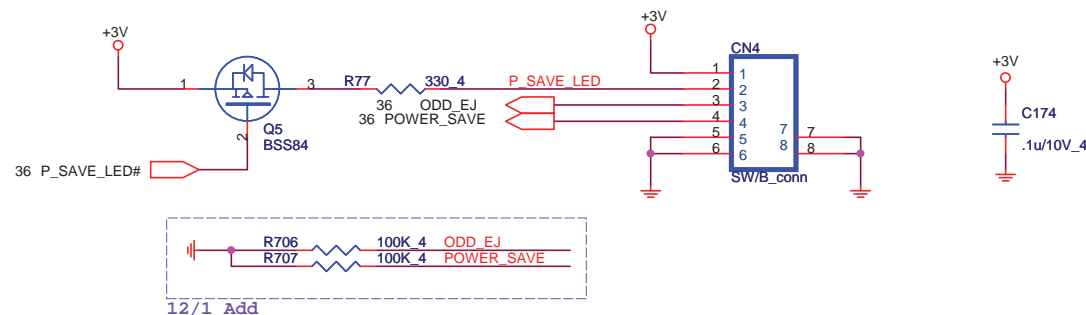
## POWER BOARD CONN(UIF)



## LED

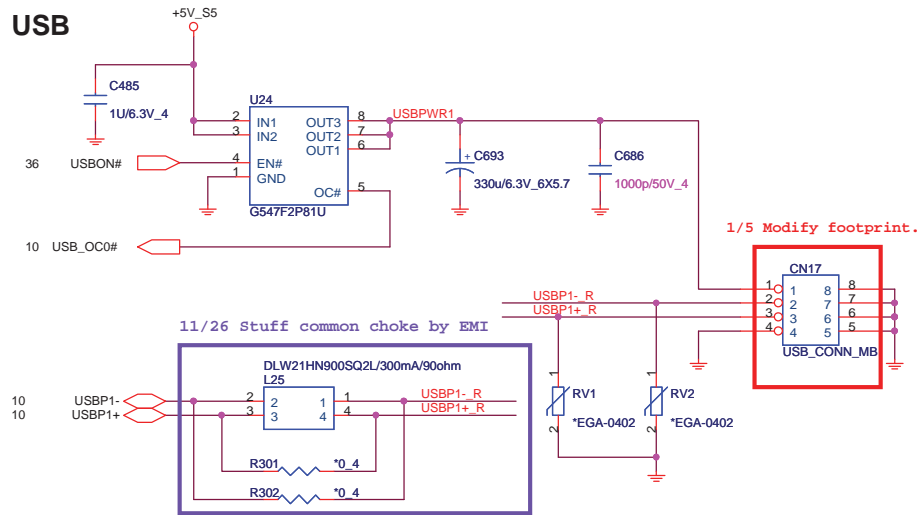


## SW /B

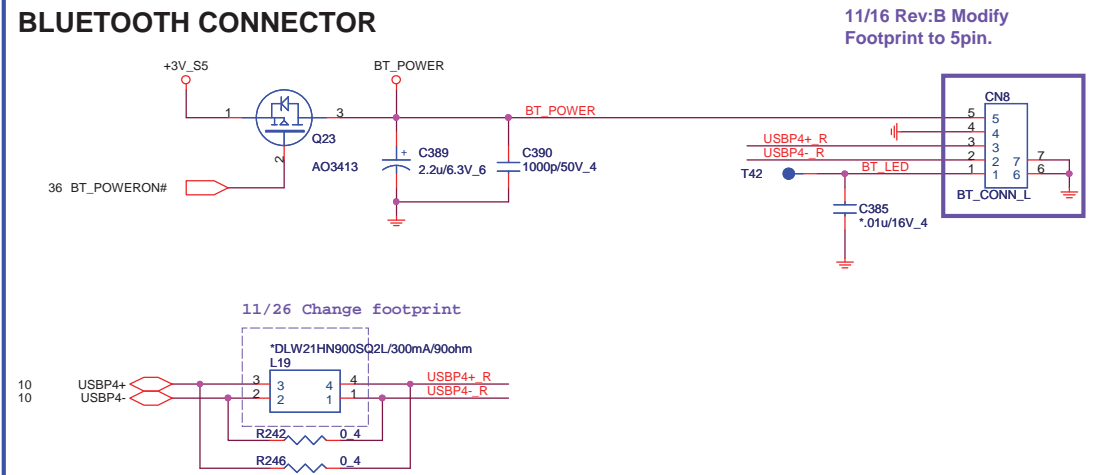




## USB

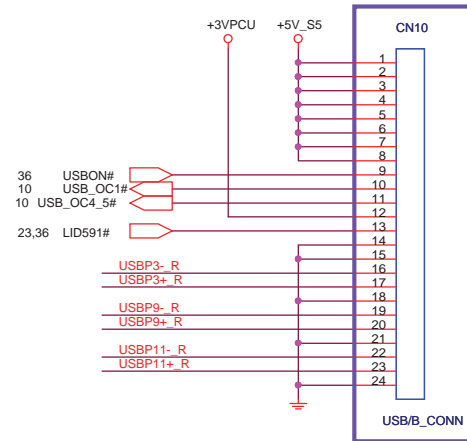
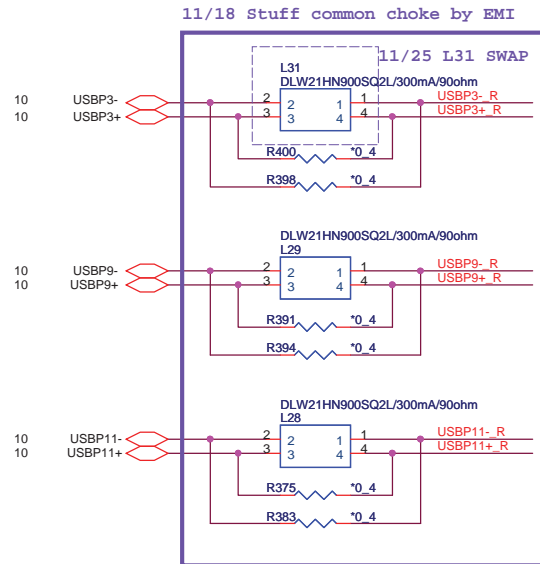


## BLUETOOTH CONNECTOR



11/16 Rev:B Modify Footprint to 5pin.

## USB/B



11/2 Rev:B Change CN10 P/N by PDC.



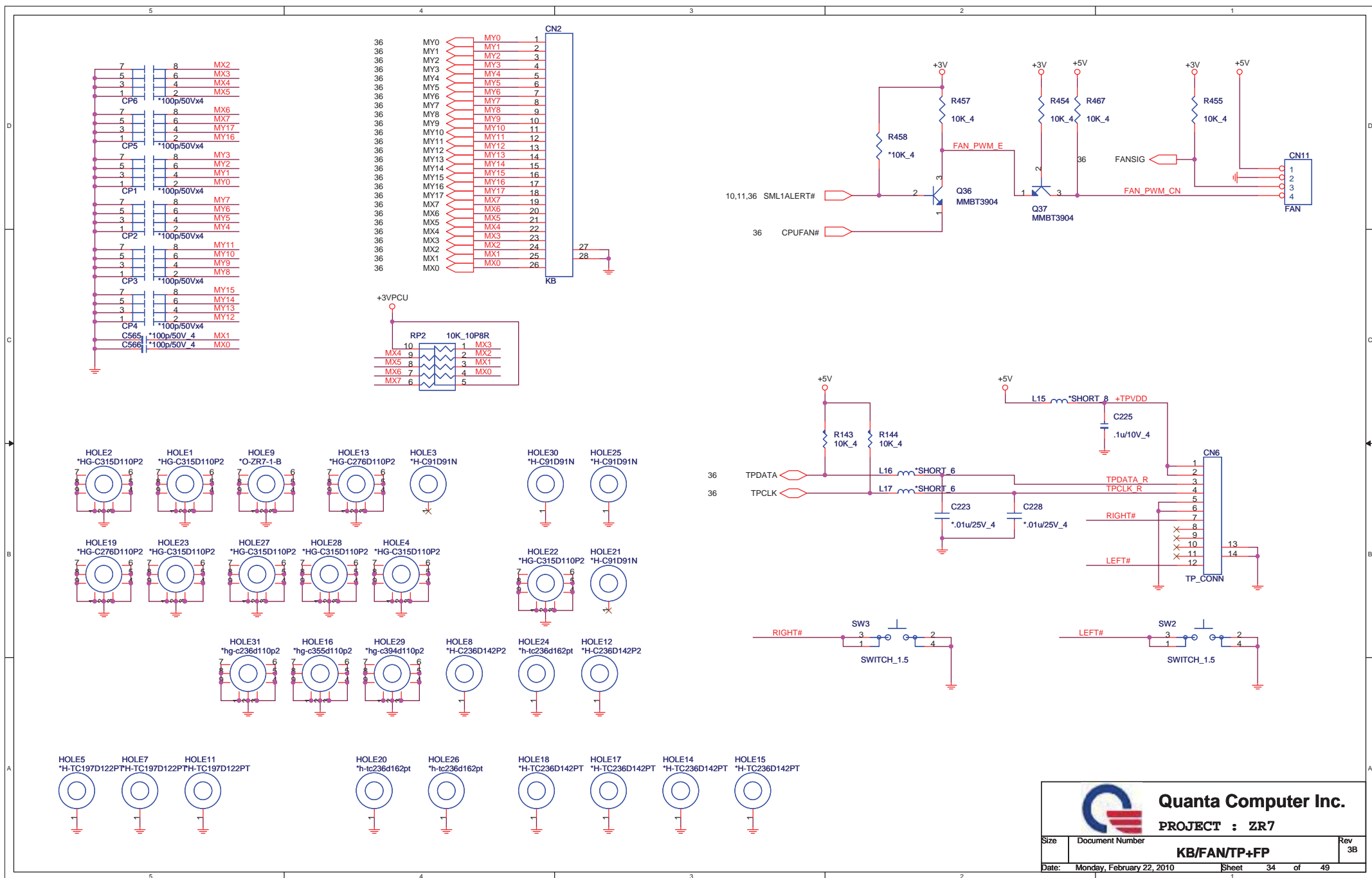
Quanta Computer Inc.

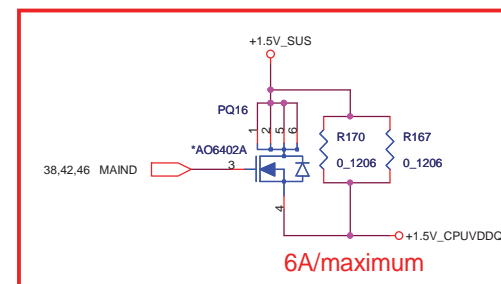
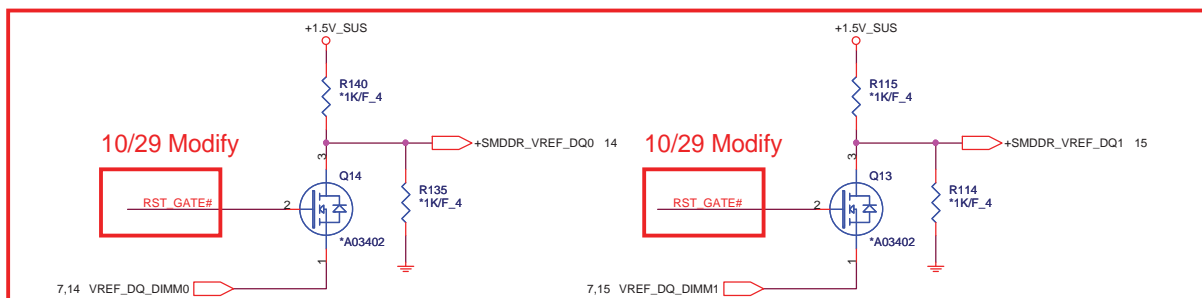
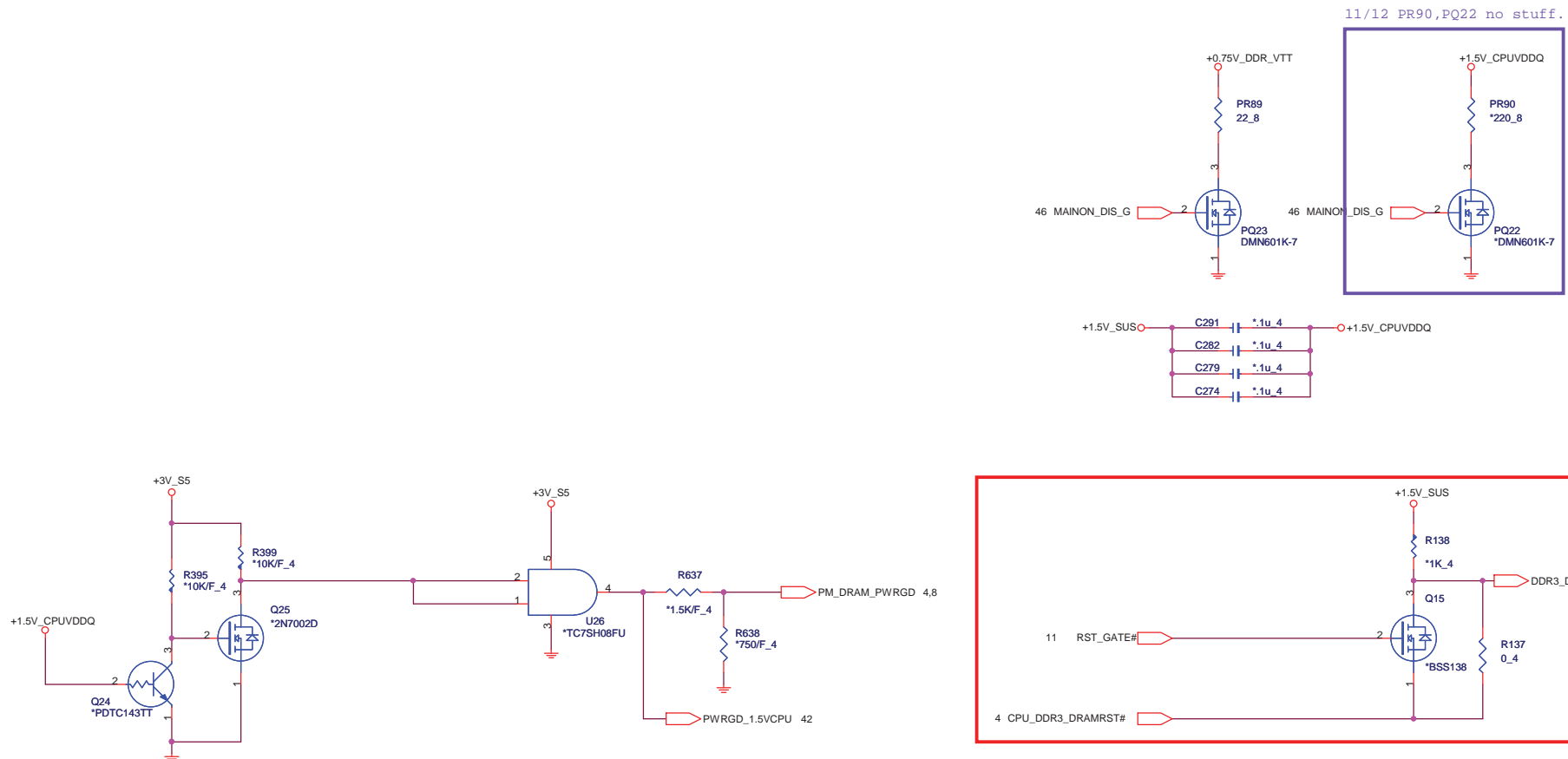
PROJECT : ZR7

USB/ BT

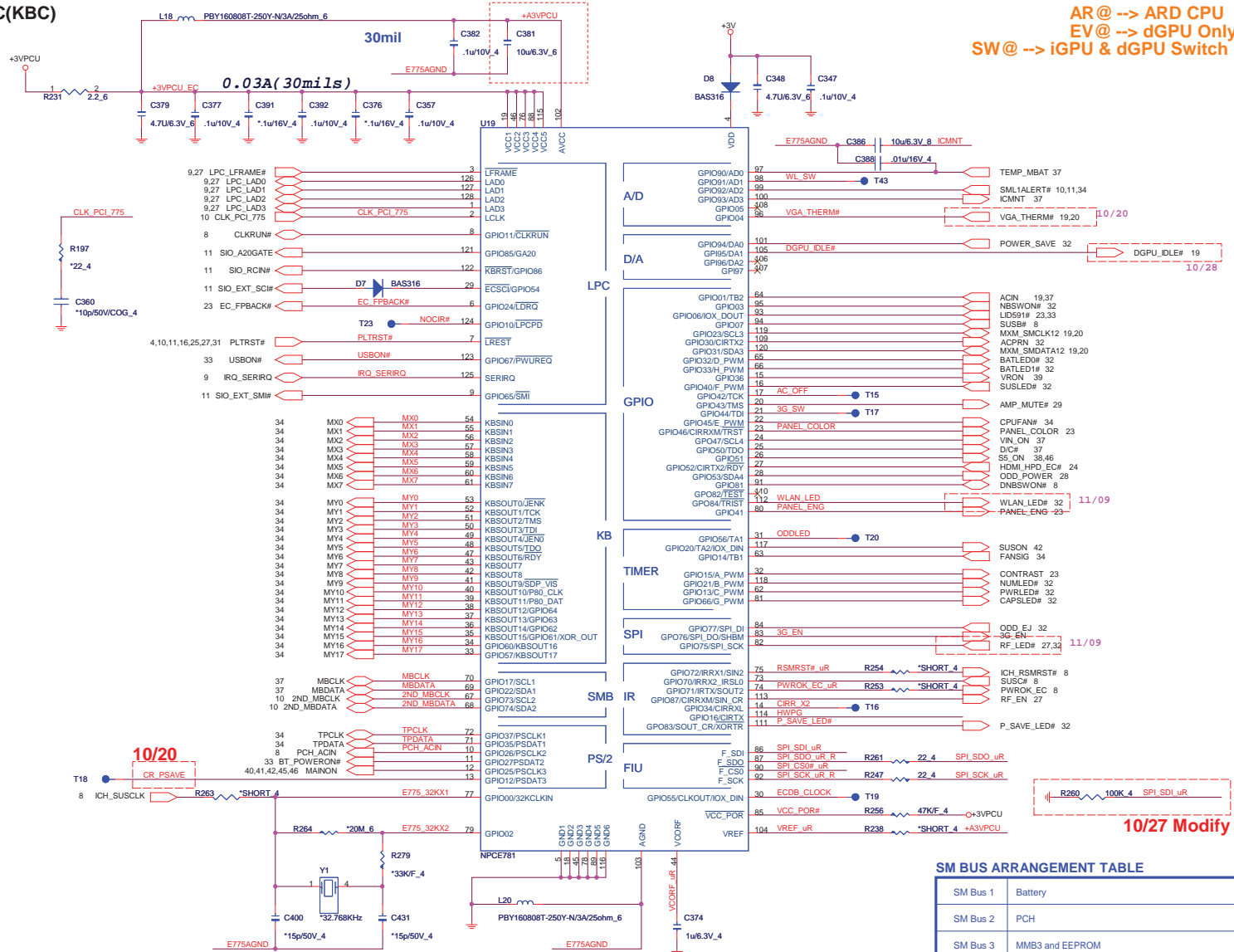
Size	Document Number	Rev
		3B

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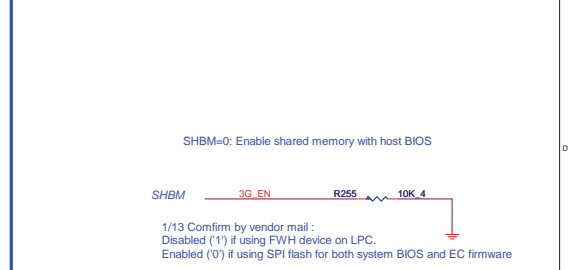




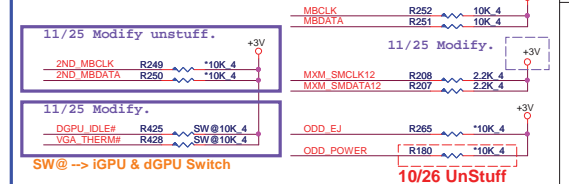
## EC(KBC)



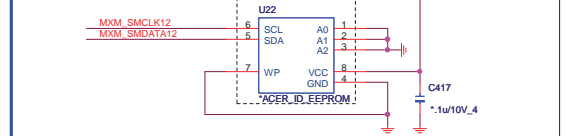
## I/O ADDRESS SETTING(KBC)



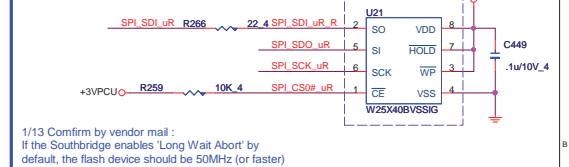
## SM BUS PU(KBC)



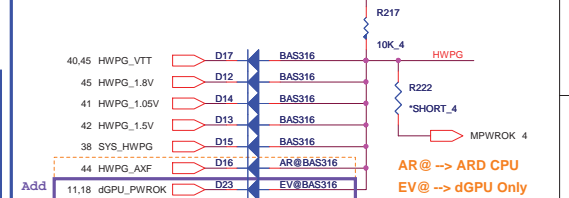
## ACER ID(KBC)



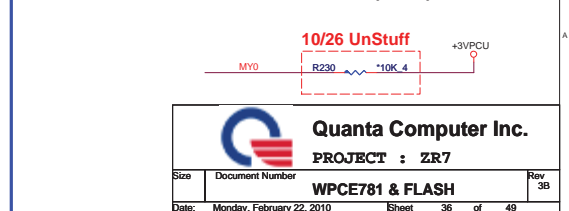
## SPI FLASH(KBC)



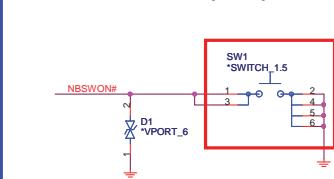
## HWPG(KBC)



## INTERNAL KEYBOARD STRIP SET(KBC)



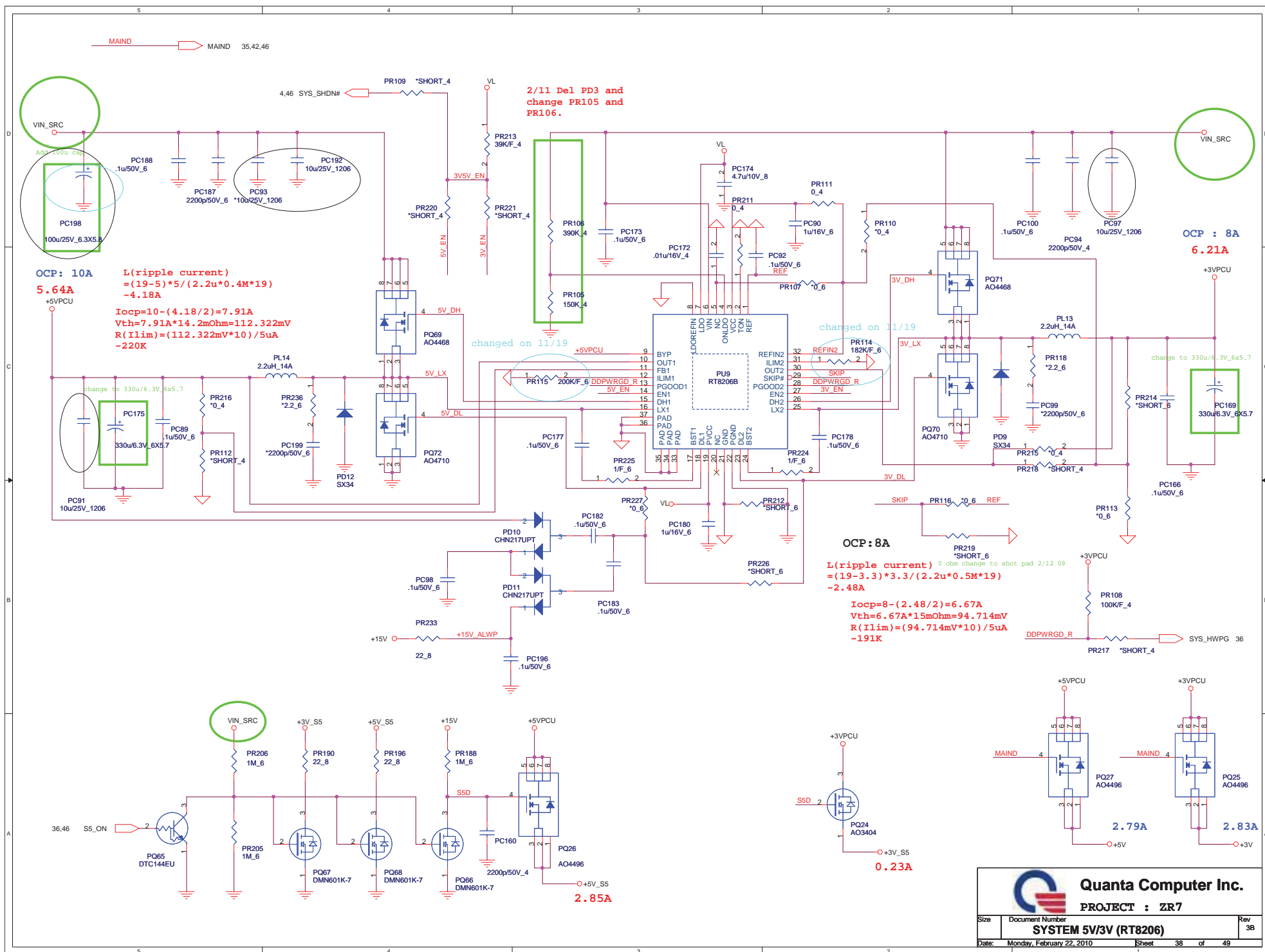
## POWER-ON Switch(KBC)



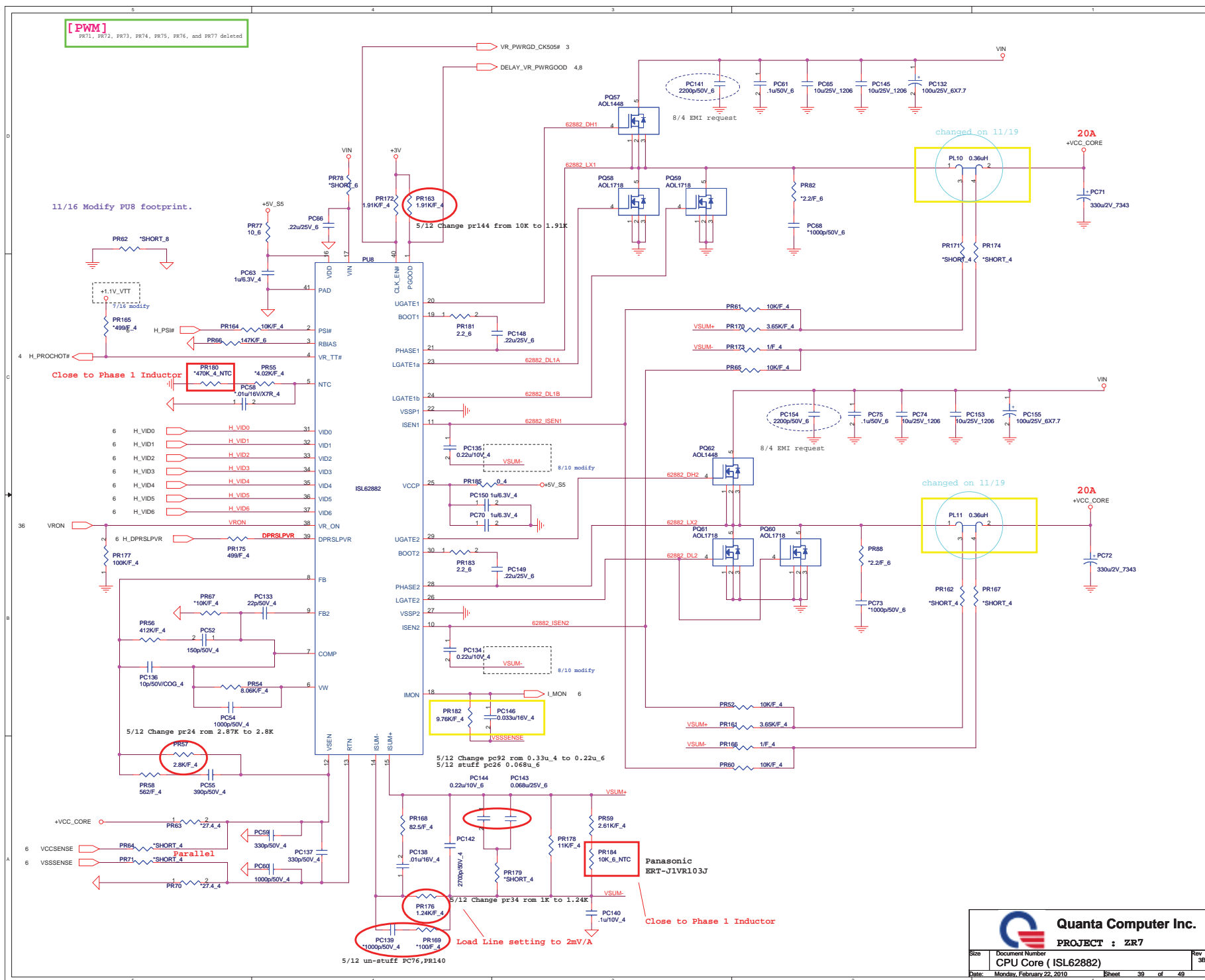
## SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	MMB3 and EEPROM
SM Bus 4	HDMI Controller, MMB1, MMB2 and VGA Thermal



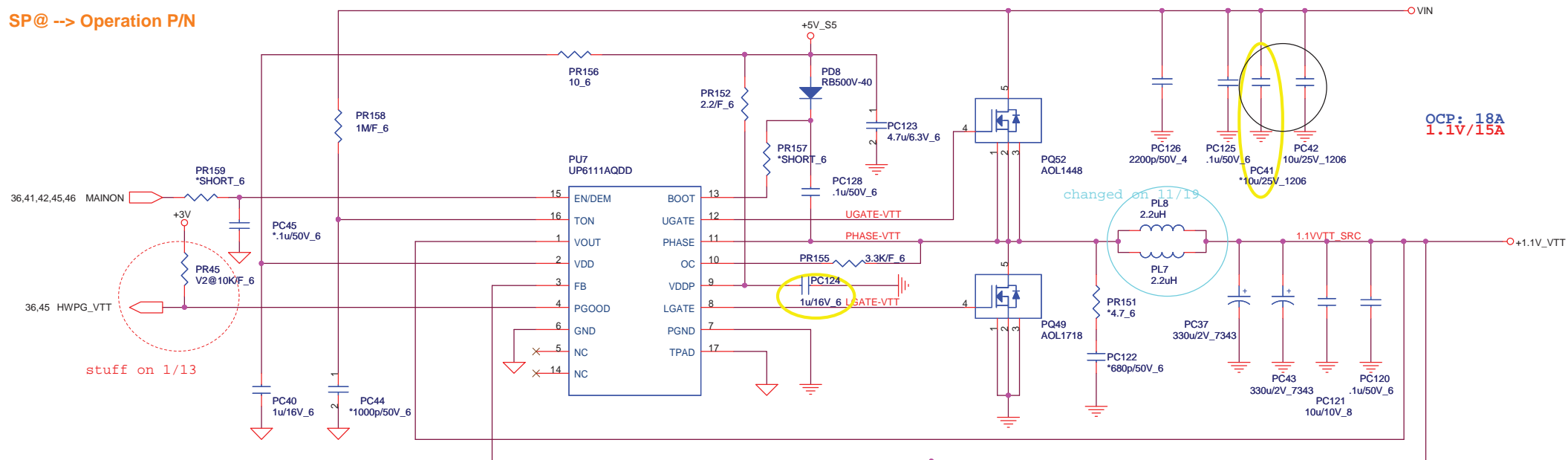






[ PWM ]

SP@ --> Operation P/N



$$V_{OUT} = (1 + R1/R2) * 0.75$$

R1 PR154 CSP@4.7K/F\_6

R2 PR153 10K/F\_6

CSP@ --> Operation P/N (ARD&CFD)

SP@ BOM change notice

Arrandale (1.05V) R1 = 4.02K (CS24023F928)  
Clarksfield(1.1V) R1 = 4.75K (CS24753F919)

$$T_{ON} = 3.85p * R_{TON} * V_{out} / (V_{in} - 0.5)$$

$$Frequency = V_{out} / (V_{in} * T_{ON})$$

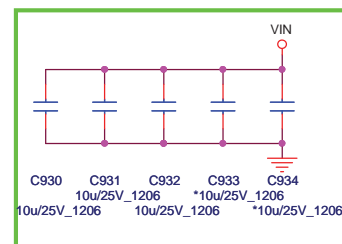
$$T_{ON} = 3.85p * 1M * 1 / (V_{in} - 0.5)$$

$$Frequency = 1 / (0.0036767) = 272K$$


A0L1718  $R_{dson} = 3 \sim 4.3m\Omega$

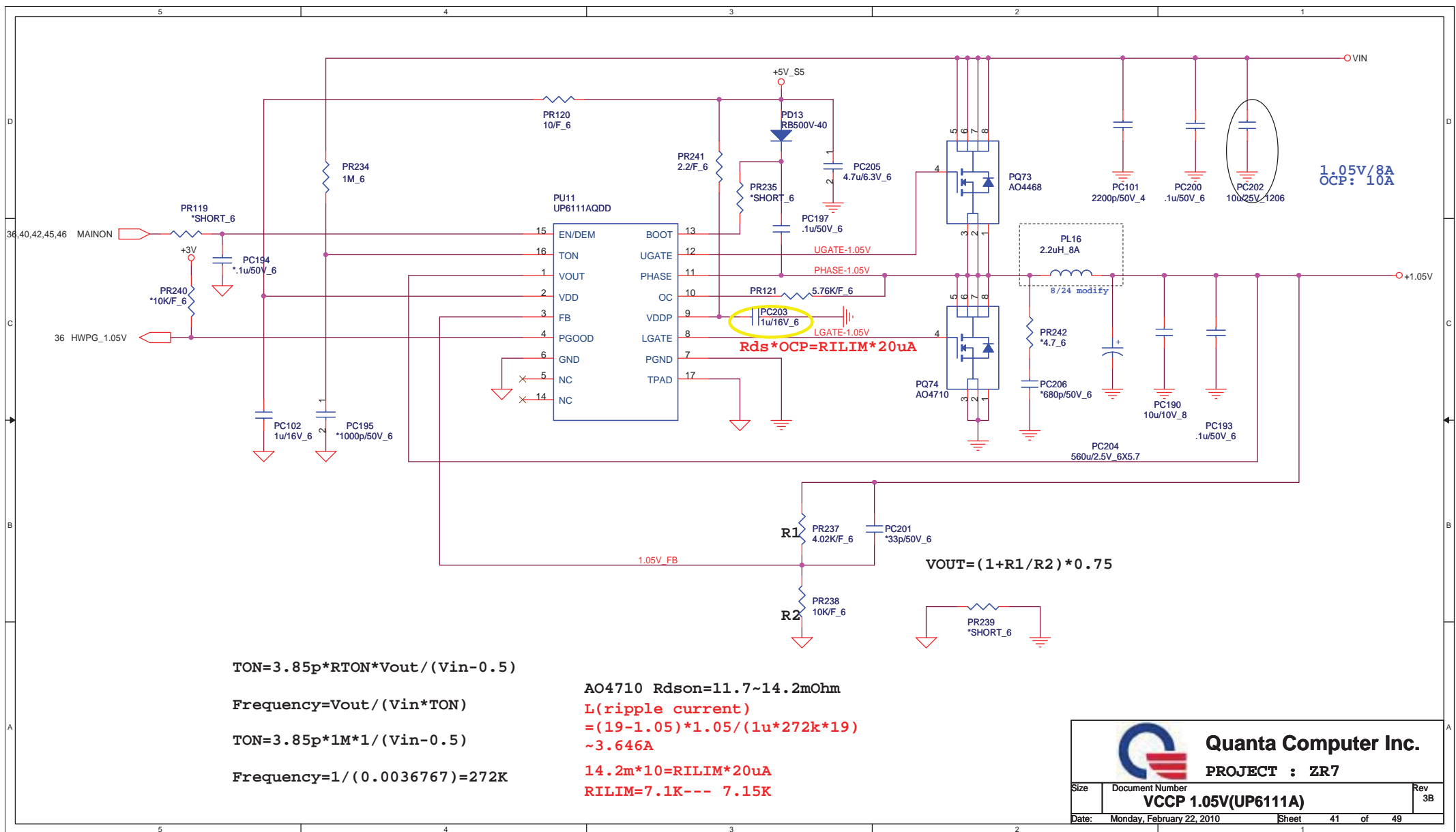
L(ripple current)  
=  $(19 - 1.05) * 1.05 / (1u * 272k * 19)$   
~3.64A

$4.3m * 18 = R_{ILIM} * 20uA$   
 $R_{ILIM} = 3.87K \text{ --- } 3.92K$

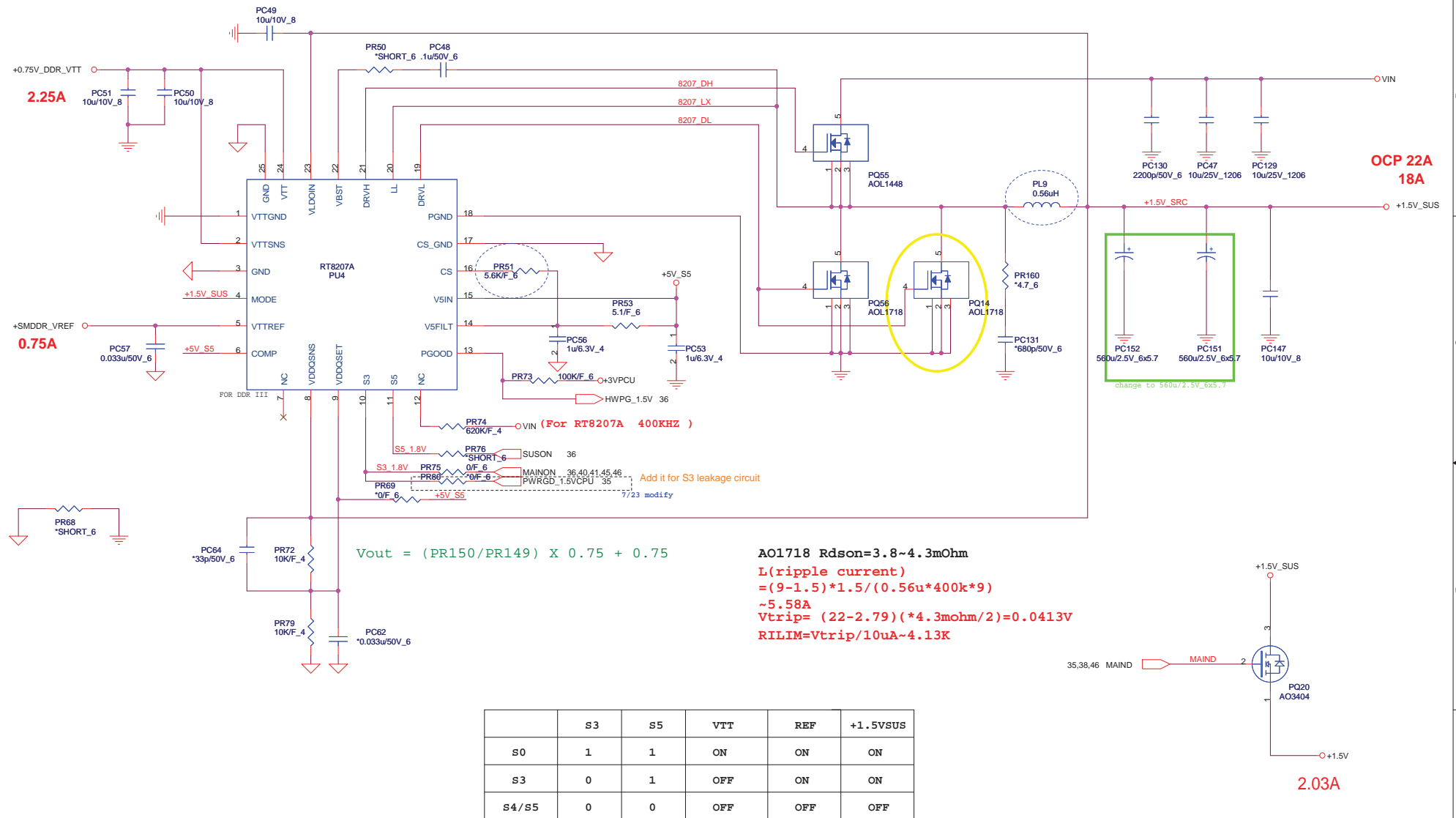


2/11 Add C930-C934 by monitor test.

 <b>Quanta Computer Inc.</b> PROJECT : ZR7		Size
		Document Number +VTT (UP6111A)
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[ PWM ]



11/16 Change VGPU\_CORE to two phase solution.

## SW@ --> iGPU & dGPU Switch

SW@ --> iGPU & dGPU Switch

11,47 dGPU\_VRON 

EV@ --> dGPU only

1/13 Add PR3032.

45,47 VGA\_PG

19,47 GPU\_VID1

11M@ -> N11M-GE1 Setitng

A horizontal number line with tick marks from 0 to 10. A purple dot is placed on the tick mark for the number 2.

```
ripple current~3.2A--> current
limit=60mV(Vcc) & Rdcr_eq=2.69mohm
-->OCP=(60mV/2.69m+3.2A/2)*2=48A
```

TDC 36A/OCP 48A  
+VGPU\_CORE

VID1

VID2

GPU_VID1	GPU_VID2	+VGPU_CORE
0	0	1.035V
1	0	0.95V
0	1	0.85V
1	1	0.8V



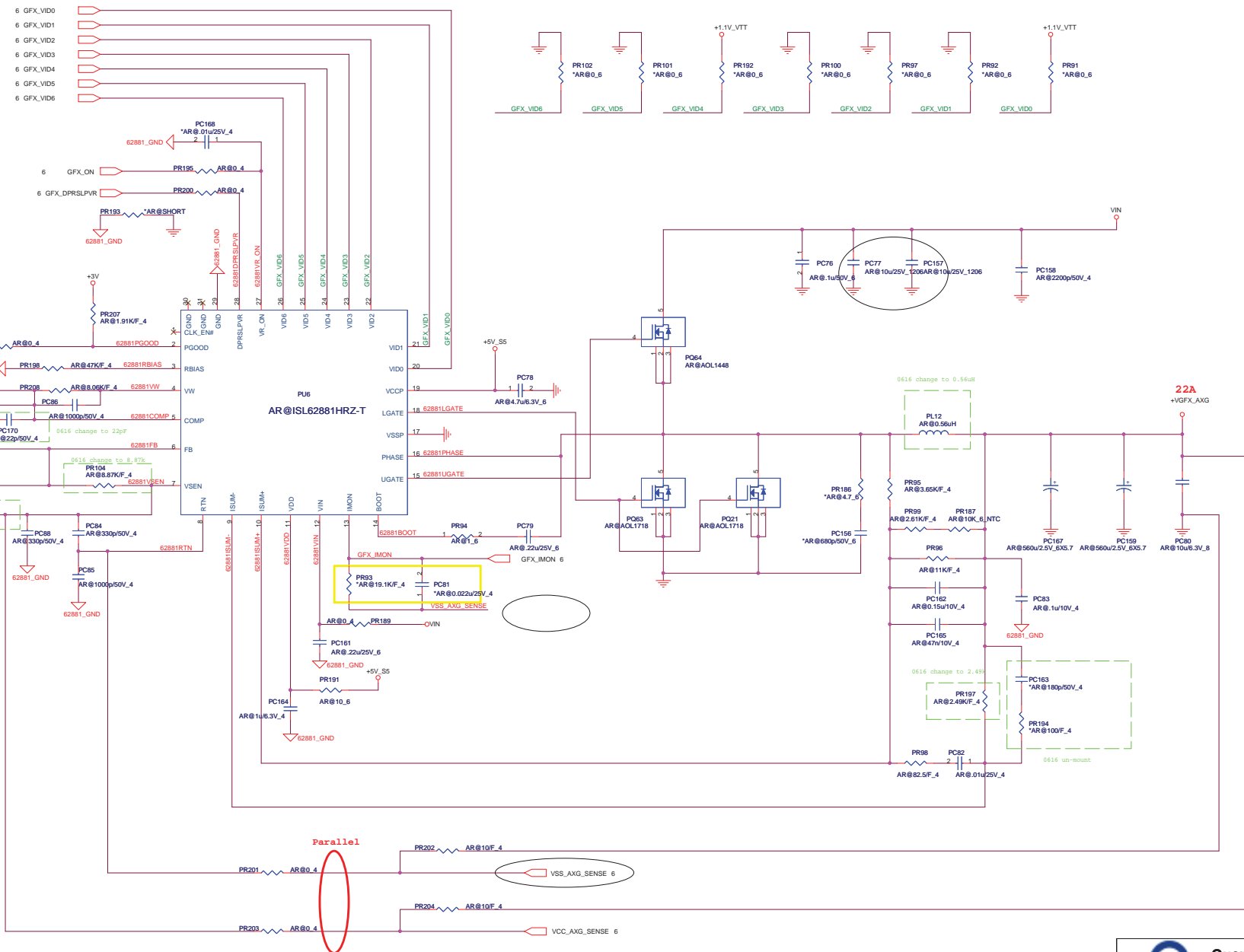
PROJECT : ZR7

Size	Document Number <b>GPU CORE(MAX17007)</b>	Rev <b>3B</b>
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# Int\_VGA [PWM]

AR@ --> ARD CPU

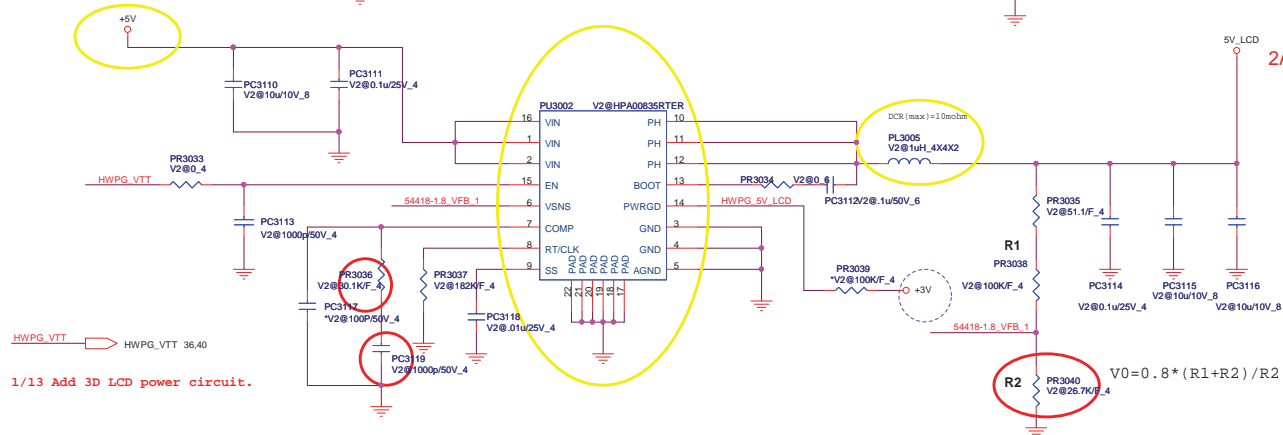
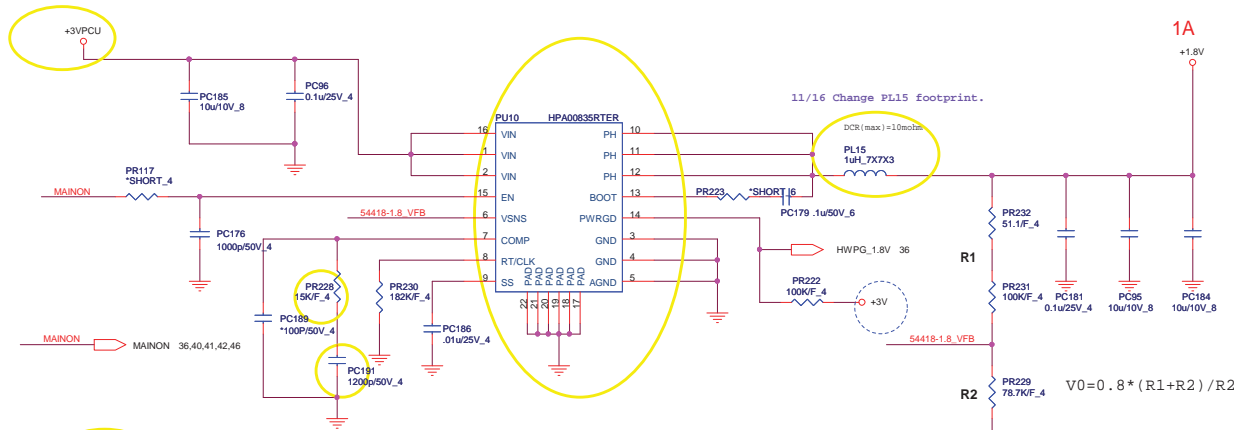
11/16 Change PU6 footprint by SMT.



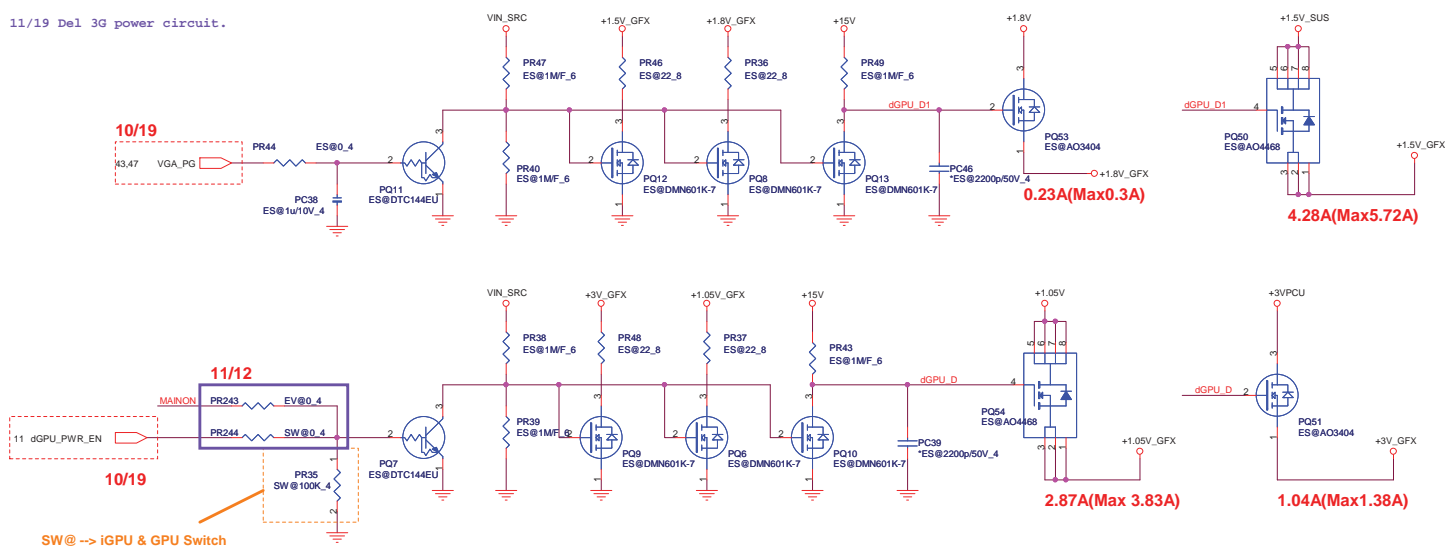
DCR=1.6~1.8mOhm  
Load Line=7mV/A  
1.6m\*0.6168=0.986m  
0.986m/.49K=396p  
392p\*2\*8.87K=7.03m  
OCF  
20u/2\*2.49K=24.9m  
24.9m/0.6168=40.3m  
40.3m/1.6m=25.2A

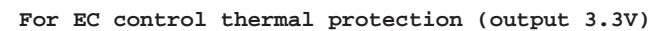


ES@ --> External VGA SKU  
SW@ --> iGPU & GPU Switch

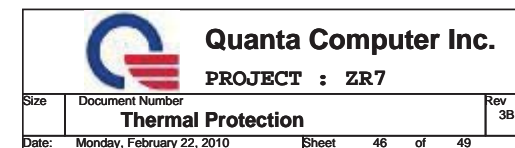


11/19 Del 3G power circuit.

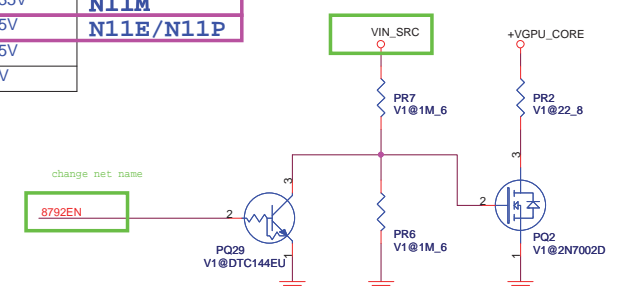


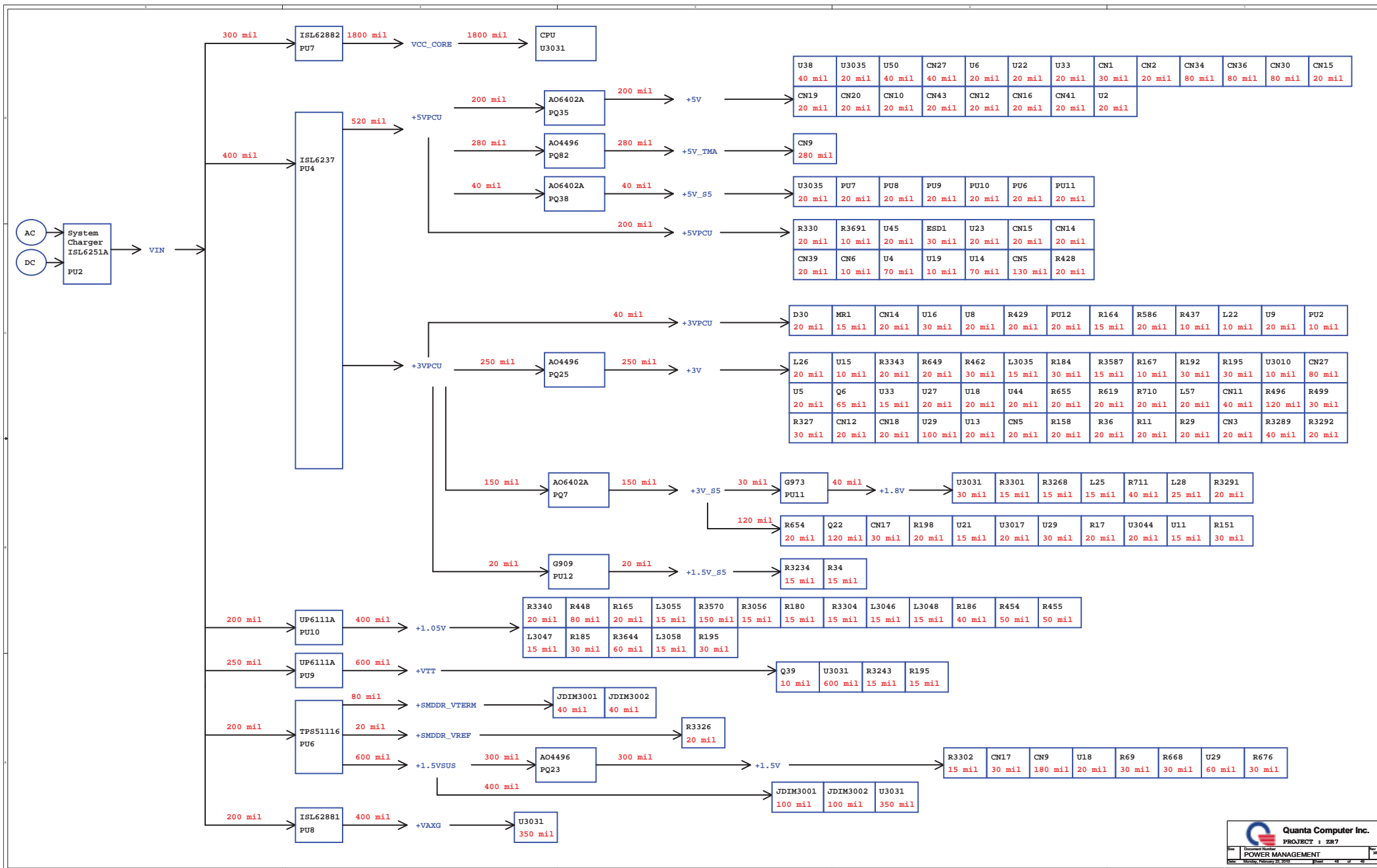


## Thermal protection




## 11P@ --> N11P-GE1 Setitng





Model		REV	CHANGE LIST	MODEL		ZR7		
				FROM	To			
ZR7 MB	2A	11/2	Page33 Change CN10 P/N by PDC.	1A	2A			
		11/5	Page9 change R338 and R594 to 10K ohm by checklist.	1A	2A			
		11/5	Page10 Add R699 connect XTAL25_IN to Gnd on EV sku and stuff Xtal components by checklist.	1A	2A			
		11/5	Page11 un-stuff R318 and del C459 and add R698 connect VCCLAN to GND by checklist.	1A	2A			
		11/9	Page32 change W/L LMD signal to control by EC.	1A	2A			
		11/9	Page36 Add EC pin82/L12 for W/L LMD control by EC.	1A	2A			
		11/12	Page35 PR90,PQ22 no stuff.	1A	2A			
		11/12	Page45 Add PR243,PR244 for option.	1A	2A			
		11/16	Page23 CMS Add LVDS signal to two channel and change CN3 to Spin conn.	1A	2A			
		11/16	Page43 GPU VCCHE power change to two phase solution.	1A	2A			
		11/16	Page27 Add CN12 Spin conn for Touch screen by ME.	1A	2A			
		11/16	Page44 Change P06 footprint by SMT.	1A	2A			
		11/16	Page45 Change PL15 footprint to CHOKER-PCMC063T-3R38M-SMT by SMT.	1A	2A			
		11/16	Page39 Change P08 footprint to qfn40-5x5-4-41p-0.75h-smt by SMT.	1A	2A			
		11/16	Page37 Change P03 footprint to QFN28-5X5-5-33P-SMT by SMT.	1A	2A			
		11/18	Page10 Delete R597, C444,C445 for cancel 3G Function.	1A	2A			
		11/18	Page10 R368,R393 modify from 47ohm to 56ohm by Realtek.	1A	2A			
		11/18	Page10 Change BOARD_ID0-2 to BOARD_ID0-3.	1A	2A			
		11/18	Page11 Change GPIO7 to BOARD_ID0 and reserve R439 PD.	1A	2A			
		11/18	Page36 Add D23 to connect to dGPU_PWRON on EV sku.	1A	2A			
		11/18	Page9 Change P/N follow ZR7B that use right angle connector.	1A	2A			
		11/18	Page27 Reserve C919, CN22 for NV IR signals on B-test.	1A	2A			
		11/19	Page1 Change U39 PN to AL00197002 by vendor.	1A	2A			
		11/19	Page31 Change CN9 footprint a P/N follow ZR7B.	1A	2A			
		11/19	Page27 Add R697 for MI-PI.	1A	2A			
		11/19	Page11 Add R442, R440 to dGPU_PWRON_R and stuff R321 on EV sku.	1A	2A			
		11/19	Page23 Modify CMS pin define.	1A	2A			
		11/20	Page43 Add PR124 on EV sku.	1A	2A			
		11/20	Page12-14 Change core logic cap .1uF CH410032R35 to CH4102K1B03 by SMT.	1A	2A			
		11/20	Page45 del 3G power circuit.	1A	2A			
		11/20	Page14 del HOLE10, Add HOLE5,HOLE6,HOLE7,HOLE8,HOLE11,HOLE12,HOLE14,HOLE15,HOLE17,HOLE18,HOLE20,HOLE24,HOLE25,HOLE26,HOLE30 P/N	1A	2A			
		11/25	Page10 Q26,Q29 change to unstuff , Add R700,R701 0 ohm for S3 leakage	1A	2A			
		11/25	Page20 C151 change to OC7343 package	1A	2A			
		11/25	Page14 Change HOLE8,HOLE12 footprint to H-C216D142P2 , Change HOLE5,HOLE7,HOLE11 footprint to H-TC197DL122PT , Change HOLE14,HOLE15,HOLE17,HOLE18 footprint to H-TC136D142PT , Change HOLE20,HOLE24,HOLE26 footprint to H-TC136D142PT , Change HOLE9 footprint to O-SMT-1-8	1A	2A			
		11/25	Page36 R425 change to dGPU_IDLEH signal and value to SW SKU , R428 change value to SW SKU , R249,R250 change to unstuff	1A	2A			
		11/25	Page28 Add C920,C921,C923,C924 0.1uF for EMI	1A	2A			
		11/25	Page33 L31 SWAP for Layout House	1A	2A			
		11/25	Page27 Modify LTRST8_7726 net name to PLTRST8	1A	2A			
		11/26	Page33 Change L19/L25 footprint , Stuff L25 common choke & unstuff R301,R302 by EMI	1A	2A			
		11/26	Page23 Change L2 footprint	1A	2A			
		11/26	Page23 Change R899,R890 to PLTR8 for EMI	1A	2A			
		11/26	Page28 Add C925,C926,C927 for EMI	1A	2A			
		11/26	Page11 Modify R422 Value to IVS SKU	1A	2A			
		11/27	Page11 Del R440	1A	2A			
		11/27	Page20 C81,C105 change OC9603 package	1A	2A			
		11/27	Page16 C84,C109 change OC9603 package	1A	2A			
		11/27	Page23 Add CMS pin45 to GND	1A	2A			
		11/27	Page27 Add L46,L47,R702,R703,R704,R705 by EMI	1A	2A			
		11/27	Page10 Modify C699,C703 to 27pF	1A	2A			
		11/27	Page18 Modify C601,C600 to 27pF	1A	2A			
		12/1	Page27 Modify CN12 to 6 pin connector	1A	2A			
		12/1	Page32 Modify LBD3 & Add R706,R707 PD by EC CDD_RJ & POWER_SAVE	1A	2A			
		12/1	Page9 Add R708,R709 by SPI ROM	1A	2A			
		3A	12/18	Page32 Add R710,R711,Q57 by EC.	2A	3A		
			12/18	Page23 Add R712,R713 by 3D feature.	2A	3A		
			12/18	Page47 Change PL6 footprint to choke-mp1136-2r2-smt by SMT.	2A	3A		
			12/29	Page27 Change CN21 footprint to MIPCI-800055F8052GX0p1-52P-smt by SMT.	2A	3A		
			12/29	Page23 Add F1 by safety.	2A	3A		
			12/29	Page24 Change Q16, Q45 P/N & add F2 by HMDI submit and safety; del U15, U16, U18.	2A	3A		
			12/29	Page10 Change CN19 color to black P/N: DPTJ08FW130 by ACM.	2A	3A		
			1/5	Page33 Change CN17 footprint to USB-UB1110C-RABED-7F-4P-8-V-SMT by PDC.	2A	3A		
			1/7	Page23 Change Q12 of dGPU_select# signal design by leakage issue.	2A	3A		
			1/7	Page9 Change BT1 P/N to DPHD02MS784 by ME issue.	2A	3A		
			1/8	Page27 Change CN12,CN22 Spin conn footprint for Touch Screen and IR.	2A	3A		
			1/11	Page23 Add L48 & stuff L2 and un-stuff R28 and R29 by EMI.	2A	3A		
			1/11	Page43 Add C928 by EMI.	2A	3A		
			1/13	Page12,36 Change C111,C182 to 10U 6.3V.	2A	3A		
			1/14	Page23 Change LVDS connector Pin4 define from NC to LCDVCC & add J3 by 3D PWR.	2A	3A		
		1/14	Page28 Change C218,C678 to 10U/10V_8 and footprint 0805.	2A	3A			
3B	2/3	Page 16-22 Change U33 footprint to fcbga973-nvidia-nlip-ee-al by NV.	3A	3B				
	2/3	Page 30 Change R368,R393 to 75ohm.	3A	3B				
		Power modify:	1A	2A				
2A	11/19	Take out JP12, JP9, JP5, JP6, JP7, JP19, JP20, JP8, JP10, JP11,JP13, JP15, JP16, JP1, JP17, JP14, JP18.	1A	2A				
	11/19	Page38 Change PC198 value; change PR14 from 191K to 182K, PR115 from 220K to 200K,PR106 from 100K to 1K,PR105 from 200K to 150K.	1A	2A				
	11/19	Page40 Change PL7,PL8 from 1.0uH to 2.2uH.	1A	2A				
	11/19	Page39 Change PL10,PL11 from DC-36TOM000 to CV-18VOM204.	1A	2A				
	11/19	Page43 Reserve PC3030.	1A	2A				
	11/23	Page37 PR19 change to 150K , PR20 change to 39K , PC112 change to 1U 25V	1A	2A				
	11/29	Page47 Change PL7,PL8,PL15,PL16 Footprint to CHOKER-PCMC063T-3R38M-SMT by SMT.	2A	3A				
	12/29	Page37 Change PR136 footprint to RC3720-SMT by SMT.	2A	3A				
	1/5	Page37-48 Change Footprint from CHOKER-ETQP4LR36WFC to CHOKER-ETQP4LR36WFC-SMT by PDC.	2A	3A				
	1/11	Page37 Add PC1300-PC1309 by EMI.	2A	3A				
3A	1/11	Page47 Change value of PQ7021,PL6,PL3004 by BCM.	2A	3A				
	1/13	Page43 Reserve PR3032 by PWR.	2A	3A				
	1/13	Page45 Reserve circuit of LCDVCC by PWR.	2A	3A				
	2/10	Page37 Reserve ECL-BC5 by EMI.	3A	3B				
	2/11	Page38 Del PD3 by power.	3A	3B				
	2/11	Page40 Add C930-C934 by monitor test.	3A	3B				
			3A	3B				
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